University of Alberta

FABRICATION OF A MICRO-PELTIER DEVICE

by

Cyrus Shafai

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Doctor of Philosophy

Department of Electrical and Computer Engineering

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To my parents

ABSTRACT

A thin film Peltier heat pump was fabricated using standard semiconductor patterning and etching techniques. The single stage Peltier pump used thin films of gold metal and bismuth telluride to form the thermoelectric junctions. The bismuth telluride films were deposited by co-evaporation of bismuth and tellurium. A study was undertaken to determine at what Te/Bi flux ratio the deposited bismuth telluride would possess the optimal resistivity and Seebeck coefficients for the Peltier device. Films deposited at a flux ratio of Te/Bi = 2.3 were found to possess the best characteristics, and these optimal films were used to fabricate micro-Peltier pumps on micromachined silicon dioxide bridges. The thermal isolation and low thermal mass of the 1.8 μm thick microbridges enhanced device performance and allowed the bulk silicon wafer to be used as a thermal reservoir. The Peltier device possessed an initial thermal response time in the cooling mode of less than 10 ms / °C, and succeeded in lowering the temperature of the microbridge 1.5 °C below ambient. This level of performance was lower than expected, and was caused by diffusion of the chrome adhesion material into the gold metal. The chrome diffusion resulted in an increase in the resistance of the gold metal and associated Joule heating, which counteracted the cooling effect of the Peltier pump. Substitution of molybdenum-tungsten as the adhesion material solved the diffusion problem. The performance characteristics of the micro-Peltier pump closely agreed with a theoretical model of the device. This model also showed temperature differentials approaching 20 °C possible with similarly constructed micro-Peltier devices. Passivation of the micro-Peltier device with a DC sputtered silicon dioxide thin film was successful. This passivation will allow for future processing steps after device construction.

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Chapter 1

INTRODUCTION

> Albert Einstein when asked to describe radio replied: "You see, wire telegraph is a kind of very, very long cat. You pull his tail in New York and his head is meowing in Los Angeles. Do you understand this? And radio operates exactly the same way: you send signals here, they receive them there. The only difference is that there is no cat."

1.1 Reason For Undertaking This Thesis

This thesis was undertaken to fabricate a thin film thermoelectric, or Peltier, heat pump small enough to allow its placement within integrated circuit (IC) devices and Micro-Electro-Mechanical Systems (MEMS). This micro-Peltier pump would be used for temperature control over select regions within the IC or MEMS. It is not intended to be used for heat sinking, as this requirement can be met with less difficulty and cost by way of thermally conducting coatings.

A Peltier heat pump[1] is a solid state device which "pumps" heat in accordance with the direction of electrical current flow through the device. Thus, a Peltier pump is capable of both heating or cooling a control surface. Presently, Peltier pumps (measuring millimeters or larger in size) are currently used in a wide variety of applications, including the active thermal control of microelectronic devices. The relatively large size of these Peltier devices compared to IC scale circuitry requires their placement on the exterior of IC packages. This adds to the size and power requirements of the Peltier device, as the

---

[1] The theory governing Peltier heat pumping is discussed in Chapter 2 of this thesis.

Peltier device must thermally regulate the IC package in addition to the electronics within it.

It is often the case that thermally sensitive elements make up only a small portion of the IC volume. In such situations, localized thermal regulation of only the thermally sensitive elements would be more efficient. The advantages of localized thermal regulation include reduced power requirements, more immediate thermal compensation, and the ability to have multiple regions within a single IC independently thermally controlled. The ability to fabricate one or more micro-Peltier pumps within IC circuitry will allow for precise and rapid localized thermal control of components within an IC.

1.2 Thermal Control Of Microelectronics And Microfabricated Devices

Active thermal control is used to stabilize the operation characteristics of a wide variety of thermally sensitive microelectronic devices. Examples of such devices are precision transistor amplifiers, laser diodes, light emitting diodes, and thermal sensing electronics. Beyond these traditional solid state devices, an increasing variety of thermally sensitive microsensors and MEMS are being implemented. Examples are microsensors for measuring gas-flow [1-5], temperature, radiation [4-11], AC power [5,12], and MEMS such as micro-calorimeters [5], nozzles for ink jet printer heads, thermally tuned resonating structures [4,13]. The small size of these devices has allowed their placement within an IC package, allowing for their integration with analysis or control electronics.

For the above devices, implementation of active temperature control typically involves heaters, heat pumps, Peltier devices, or heat sinks of various types placed on the exterior of the IC package or on the die surface within the IC package itself. For localized on-chip thermal control, resistive heaters are placed in close proximity to the microsensor or MEMS.

The recent maturing of micromachining technology has resulted in the use of thin film microstructures (such as bridges, diaphragms, or cantilevers) as thermal isolation platforms, upon which are fabricated microelectronics, microsensors, and MEMS. An example of a device fabricated on a microstructure is shown in Figure 1.1. Microstructures

are typically fabricated using silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) thin films, as these dielectric materials possess low thermal (and electrical) conductivities. The combination of the low thermal conductivity and low thermal mass of the microstructure provides three primary advantages. First, the thermal sensitivity of devices fabricated on the microstructure is greatly enhanced. Second, the microstructure responds very quickly to thermal input from resistive heaters fabricated on them. Third, the power requirement of a resistive heater on the microstructure is greatly reduced.

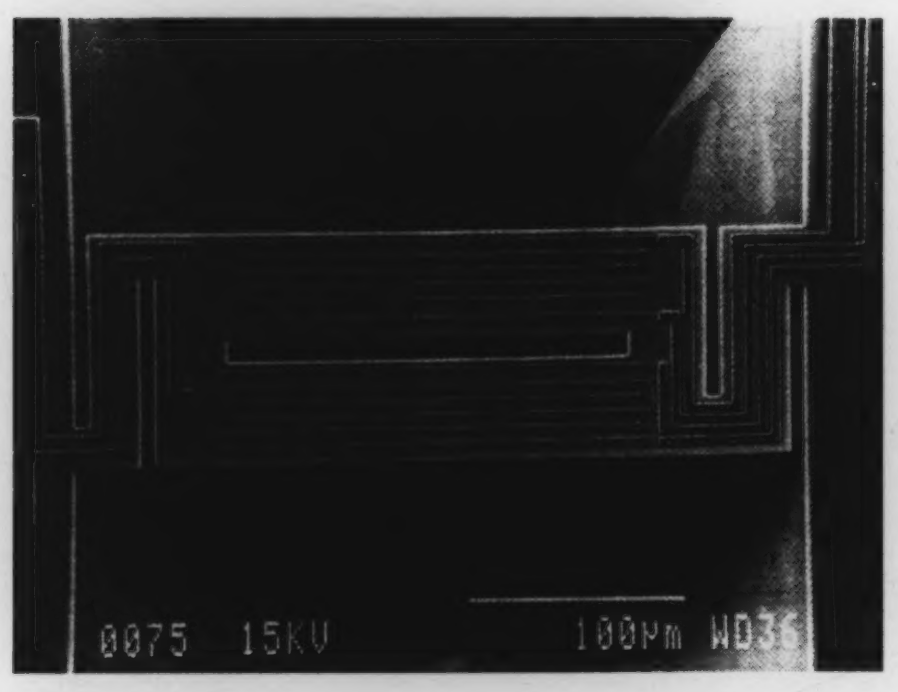

Figure 1.1: SEM picture of a microbridge gas-flow sensor fabricated using 2 µm CMOS technology [2]. Three polysilicon resistors are located on the microbridge. The middle one acts as a heating resistor. The other two are sensing elements.

A trade off does exist, however, between the thermal isolation and the thermal relaxation time (or thermal sensitivity) of a microstructure. The more thermally isolated a microstructure is, the more time it needs to recover (to the ambient temperature) from a thermal input. The solution to this problem is to have some method of active heat pumping available to accelerate the thermal relaxation time. Active heating of microstructures has been achieved with resistive heaters. However, techniques for active cooling are presently not being implemented.[2]

1.3 The Micro-Integrated Peltier Heat Pump

The micro-Peltier heat pump fabricated in this thesis is small enough to allow its placement on a thermally isolated microstructure. The two-way heat pumping ability (both heating and cooling) of the micro-Peltier pump enables its use as an active thermal control unit for the microstructure. This capability provides three benefits over the existing thermal control provided by resistive heaters fabricated on a microstructure.

1. A decreased thermal relaxation time for thermally isolated microstructures.

2. The possibility of a microstructure to exist at a temperature below ambient.

3. A power saving over existing techniques of IC die or package cooling.

---

[2] Active cooling can be effectively implemented by resistive heating. A heater would first thermally bias the microstructure (raise it above ambient temperature). Then, by varying its power, the heater will vary the microstructure temperature about the thermal bias temperature. However, this technique has the disadvantages of increased power consumption, higher thermal losses due to the above ambient bias temperature, and the requirement of operation at an elevated temperature.

Operation above ambient temperature can be avoided by using a two-stage heat pumping system. In this system, heaters provide active thermal control to the microstructure, while a bulk heat pump is used to lower the entire die or IC package below ambient temperature. However, this two-stage system requires significantly more power.

Benefit 1 is realized because the micro-Peltier pump can actively pump heat away from a microstructure, thus decreasing the thermal relaxation time of microstructures possessing a high degree of thermal isolation. This negates the aforementioned compromise between the thermal isolation and the thermal relaxation time of a microstructure. Benefit 3 is realized because the micro-Peltier device can provide localized cooling to a microstructure. Currently, a bulk heat pump is required to lower the entire die or IC package below ambient temperature. This is more energy demanding.

The design chosen for the micro-Peltier pump is that of a two-junction thermoelectric heat pump (see Figure 1.2). In this design, the Peltier pump is fabricated on one side of a SiO_2 microbridge. The thermally controlled junction of the Peltier pump is isolated on the microbridge, while the opposite junction is positioned off the microbridge and on the bulk silicon wafer. The larger thermal mass of the silicon wafer allows its use as a heat sink/source for the Peltier pump. Also shown in this figure is a possible location for the placement of a thermally controlled device at the center of the microbridge. More will be said regarding possible applications for the micro-Peltier pump in Chapter 5.

1.4 Fabrication Considerations

The practical placement of the micro-Peltier pump upon a thermally insulated microstructure requires that the pump be of a physical size on the order of the microstructure itself. Typical dimensions would be 10's to 100's of μm in length or width. Furthermore, the thickness of necessary materials should be on the order of 1-10 μm. This small physical size necessitates the use of microfabrication techniques for the micro-Peltier pump's fabrication. Specifically, techniques commonly used in the microelectronic industry are preferred as the Peltier pump is intended to be fabricated alongside microelectronics, microsensors, and MEMS. A detailed discussion of the fabrication of the micro-Peltier pump is given in Chapter 3. However, a brief description is provided below.

SiO_2 deposited by plasma enhanced chemical vapour deposition (PECVD) is used as the structural material for the microbridge. This oxide is annealed in a nitrogen

ambient to reduce stress, thus minimizing bending of the microbridge after its formation. The micro-Peltier pump is fabricated using two materials, which are electrically insulated from each other by a second PECVD SiO_2 layer. The first material, that of the wiring contacts (see Figure 1.2), is gold metal deposited by sputtering. Various device prototypes utilized chrome, nichrome, or molybdenum-tungsten metals on both sides of the gold as adhesion materials between the gold and the surrounding SiO_2 layers. The second material, bismuth telluride (Bi_2Te_3), is deposited by co-evaporation of bismuth and tellurium. Bi_2Te_3 is a semiconductor and is commonly used in many thermoelectric devices. Contacts between the two materials are made through vias in the second PECVD SiO_2 layer.

The deposited Bi_2Te_3 thin film is photolithographically patterned and subsequently etched to form necessary circuitry. It is then passivated by a sputtered SiO_2 thin film. The processes of patterning, etching, and passivating the Bi_2Te_3 film demonstrates the ability to incorporate the micro-Peltier pump alongside other IC scale devices.

A picture of a completed micro-Peltier pump fabricated on a 1.8 μm thick SiO_2 microbridge is shown in Figure 1.3. The microbridge measures 570 x 270 μm, the chrome-gold-chrome metallization is 500-1500-500 Å thick, and the Bi_2Te_3 film is 1.1 μm thick. A performance analysis of this particular device is given in chapter 4 of this thesis.

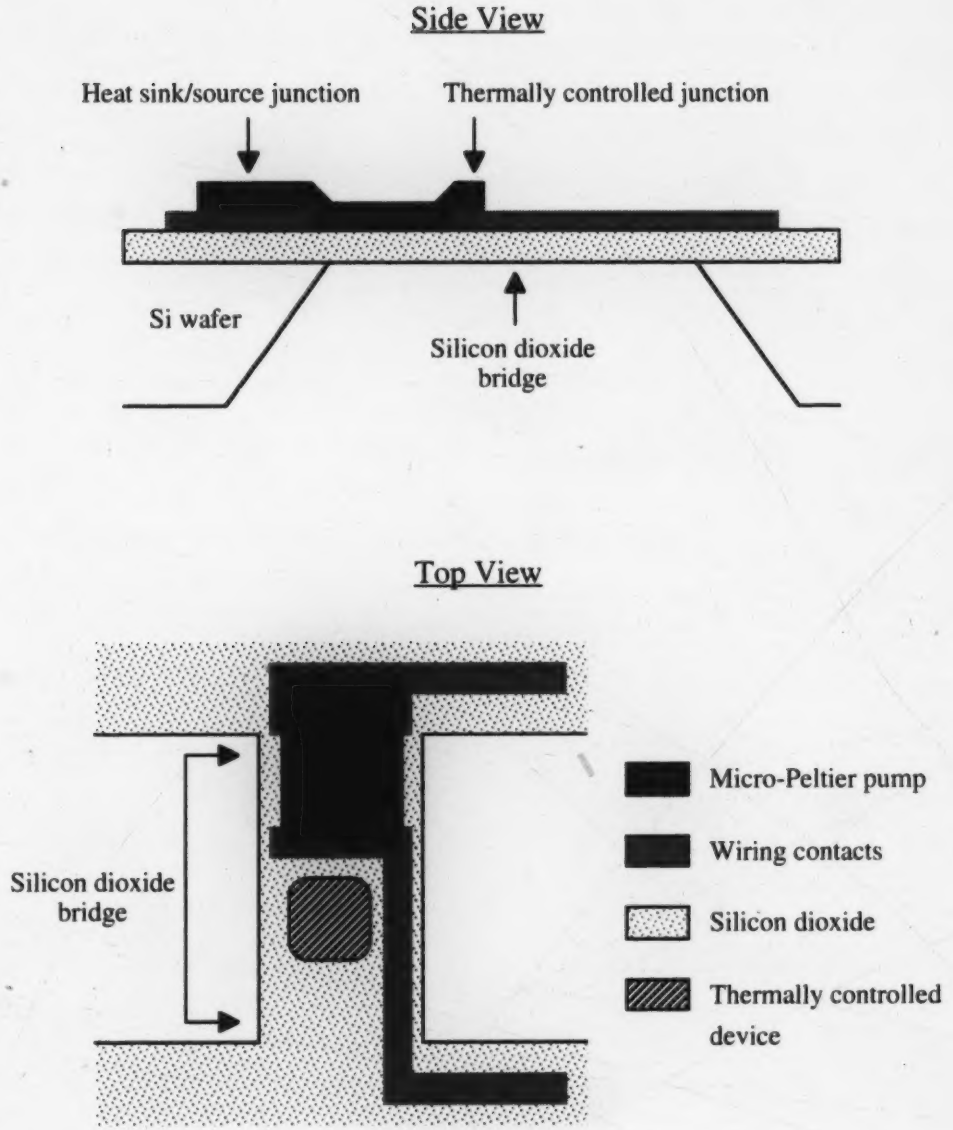

Figure 1.2: Schematic of the micro-Peltier pump fabricated on a silicon dioxide microbridge.

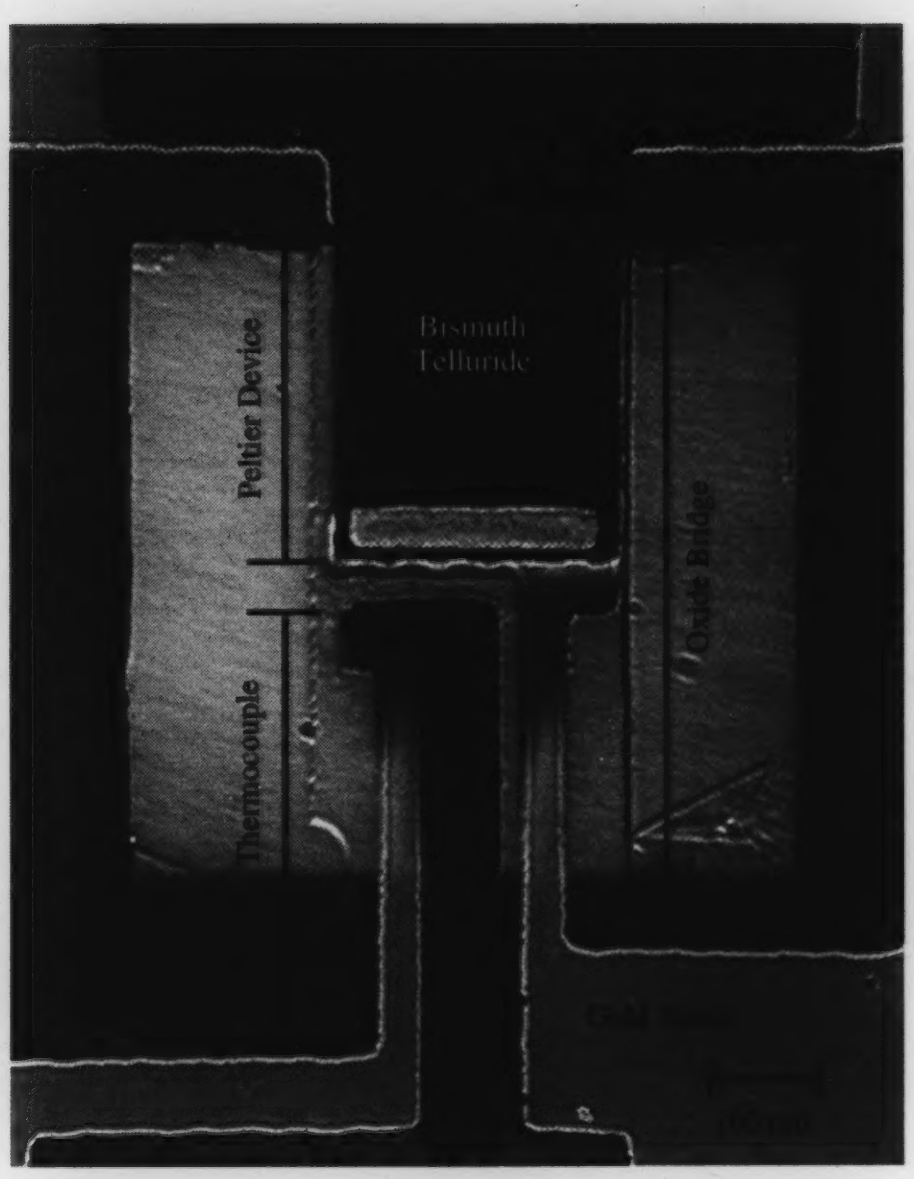

Figure 1.3: A micro-Peltier pump fabricated on a SiO_2 microbridge measuring 570 x 270 μm. A thermocouple fabricated on the microbridge is used to measure the temperature differential produced by the Peltier pump.

1.5 Scope Of This Thesis

- Chapter 2 introduces the reader to the various thermoelectric effects, Peltier heat pump theory, and thermal conductivity. This is followed by a discussion of thermoelectric materials for use in Peltier heat pumps.

- Chapter 3 discusses the fabrication of the micro-Peltier pump. Design considerations, material selection, deposition and processing, and many fabrication problems are described.

- Chapter 4 presents performance measurements for various micro-Peltier pumps. These results are compared with simulations based on the theoretical performance of the materials selected for the micro-Peltier pump.

- Chapter 5 describes possible applications for the micro-Peltier pump. Fabrication specifics for each implementation of the micro-Peltier pump are given.

- Chapter 6 presents conclusions and possible design modifications that should be investigated to improve the performance of the micro-Peltier pump.

Chapter 2

THERMOELECTRIC EFFECTS, HEAT CONDUCTION, AND A PRACTICAL PELTIER DEVICE

"Imagination is more important than knowledge."
-- Albert Einstein

2.1 Introduction

A practical Peltier heat pump should be of a design which minimizes thermal losses to the environment, and should include materials which are efficient at "pumping" heat and possess a low thermal conductivity. These latter two requirements are for many materials mutually exclusive. Before entering into a discussion as to why this is the case, the reader must possess an understanding of the thermoelectric effects and of thermal conductivity.

This chapter introduces the reader to the various thermoelectric effects and to thermal conductivity in solids. This introduction assumes the reader has had no previous contact with the subject matter. Following this, an explanation as to how a Peltier heat pump works and equations governing its operation are given. Next, a discussion of what constitutes a "good" thermoelectric material for a Peltier heat pump is provided along with criteria for material selection. Finally, heat transfer by means of thermal convection and radiation is discussed.

2.2 The Thermoelectric Effects

The thermoelectric effects are concerned with the direct conversion of heat into electrical energy or the reverse, in solid or liquid conductors. They are described by three interrelated and thermodynamically reversible effects; the Seebeck effect, the Peltier effect, and the Thomson effect. A detailed thermodynamic discussion of these effects will not be given, as it is beyond the scope of this thesis. It should be noted that Joule heating is not considered one of the thermoelectric effects due to its irreversible nature.

2.2.1 The Seebeck Effect

In 1821 T. J. Seebeck (1770 - 1831) after observing the deviation of a compass needle in the proximity of thermocouples, concluded that substances are magnetized in the presence of a thermal gradient. He described this phenomenon as "the magnetic polarization of metals and ores produced by a temperature difference" [14]. He was mistaken in that there was no magnetic effect, but he dogmatically refused to believe this was the case and fought actively against it for several years, his ultimate aim being an attempt at explaining the magnetization of the earth by reference to the thermal gradient between the poles and the equator [15]. What he actually discovered has nonetheless become known as the Seebeck effect.

The Seebeck effect is the creation of a voltage across a conductor when the ends of the conductor are held at different temperatures. This voltage is proportional to the temperature difference between the conductor ends.

The Seebeck effect can be explained by considering the effect of imposing a temperature gradient along the length of a conductor. Initially the conductor possesses a uniform charge distribution along its length, however, the hot end will have more high energy electrons than the cold end. As the diffusion rate of electrons in the conductor is a function of energy, more electrons from the hot end will diffuse towards the cold end than will diffuse from the cold end to the hot end. This causes a build up of charge at the cold end, which results in an emf in opposition to the flow of charge carriers towards the

cold end. Eventually, the magnitude of the back emf is sufficient to prevent the further flow of charge carriers. The open circuit voltage at which this occurs is called the Seebeck voltage and is given by,

$$V = \alpha \Delta T \quad \text{volts} \tag{2.1}$$

where α is the absolute Seebeck coefficient of the conductor and has the units V/K, and ΔT is the temperature difference between the conductor ends in Kelvin. It is assumed in Equation (2.1) that α is constant with temperature, which is not the case, but can be approximated as being so for small temperature variations. Taking into account temperature variations, a more correct form of Equation (2.1) would be,

$$V(T_0, T_1) = \int_{T_0}^{T_1} \alpha(t)\, dt \quad \text{volts} \tag{2.2}$$

The Seebeck coefficient is also called the thermoelectric power. Its value can be either polarity depending on the material. The Seebeck coefficient is small in most metals, typically a few microvolts per degree Kelvin. Semiconductors typically have much larger Seebeck coefficients, in the range of 100's or 1000's of μV/K. The Seebeck coefficient is negative for n-type semiconductors, and positive for p-type semiconductors. It is zero for superconductors.

The Seebeck coefficient is the sum of two terms [16],

$$\alpha = \alpha_d + \alpha_g \tag{2.3}$$

where α_d is the electron-diffusion component, and α_g is the phonon-drag component.

The variation of α with temperature can be considerable. As this thesis is concerned with the operation of a Peltier device over small temperature differences about room temperature, the variation of α with temperature will not be considered in detail. However, in the interest of completion, it will be discussed briefly below.

At absolute zero the Seebeck coefficient is zero. As the temperature is increased, α typically rises very rapidly, reaches a maximum, then drops off (see Figure 2.1). This

rapid variation is due to a rapid increase and then drop in α_g with temperature. With further increasing temperature, α again increases in magnitude with the increase in α_d due to more electrons being available as charge carriers. Typically, α_d is slowly varying with temperature and it is the dominant effect at room temperature (300 K) and above.

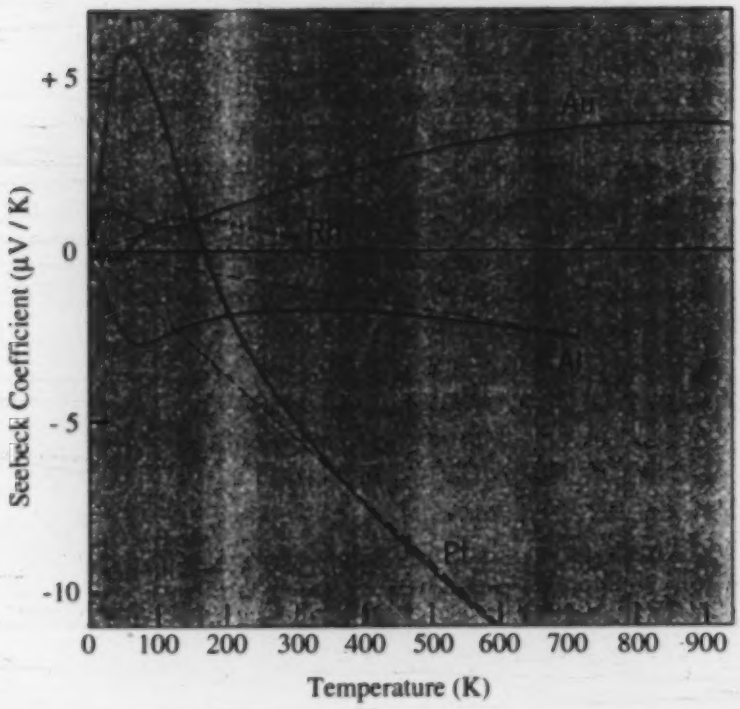

Figure 2.1: The solid curves indicate the total Seebeck coefficients of gold (Au), aluminum (Al), platinum (Pt), and rhodium (Rh) as a function of temperature. The differences in the solid curves and the broken lines for Pt, Al, and Au indicate the magnitude of the phonon-drag component [16].

The reason for the rapid variation in α_g in Figure 2.1 is due to the change in the type of phonon scattering with temperature. At low temperatures, phonon-electron scattering is more significant than phonon-phonon scattering. Phonons diffusing through a conductor will drag electrons along. As the temperature is increased from absolute zero, an increasing number of phonons are available to drag electrons, resulting in an increase in α_g. However, as the temperature increases, phonon-phonon scattering becomes dominant and fewer electrons are pulled along. Consequently, α_g drops off in magnitude.

2.2.2 The Relative Seebeck Coefficient

When two dissimilar conductors are subject to an identical temperature difference across their lengths (see Figure 2.2), a voltage can be measured between the free ends of the conductors. This voltage is the difference of the open circuit Seebeck voltages of the two conductors, and is given by,

$$V = \alpha_{AB} \Delta T \quad \text{volts} \tag{2.4}$$

where α_{AB} is the difference of the absolute Seebeck coefficient of the two conductors, and is called the relative Seebeck coefficient.

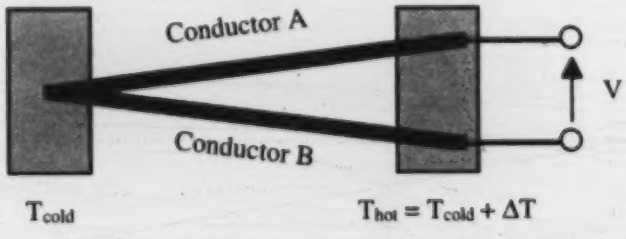

Figure 2.2: The relative Seebeck effect.

It is assumed in Equation (2.4) that α_{AB} is constant with temperature. More generally,

$$V(T_0, T_1) = \int_{T_0}^{T_1} \alpha_{AB}(t)\, dt \quad \text{volts} \tag{2.5}$$

The magnitude of this voltage has been shown to be solely a function of the temperature difference between the ends of the conductors, and upon the conductor materials. It is independent of all other variables, including changes in conductor cross-section, intermediate temperature distributions, or large local temperature gradients. This effect has been harnessed to generate electrical power, and has found use in thermocouples to measure the temperature difference between two regions.

2.2.3 The Peltier Effect

In 1834 J. C. A. Peltier (1785 - 1845), a watchmaker, discovered the complimentary effect to the Seebeck effect. Peltier himself did not recognize the connection with the Seebeck effect, and sought an explanation of this effect in the hardness or softness of the metal or its electrical conductivity. It was not until 1838 that Lenz put an end to all doubts regarding the true nature of the Peltier phenomenon [14].

Peltier discovered that when an electric current crosses the junction between two dissimilar conductors, heat is absorbed or liberated at the junction (see Figure 2.3). If the direction of current flow is reversed, the effect also reverses.

This symmetry is illustrated in Figure 2.3 (It is assumed that materials A and B possess uniform thermal mass.). Electric current (traveling from left to right) absorbs energy when crossing the junction from material A to B, and decreases the junction temperature by ΔT. By symmetry, the current releases energy when crossing from B to A, increasing the junction temperature by ΔT. Conservation of energy is satisfied in the Peltier effect.

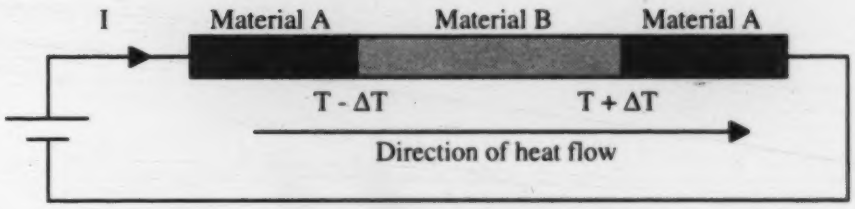

Figure 2.3: The Peltier effect.

The Peltier effect arises because the average energy of the charge carriers within dissimilar materials is different. Therefore, when crossing from one material to another, a charge carrier must interchange energy with the surroundings at the junction in order to maintain conservation of energy within the new material. This effect is independent of the magnitude of the current, and shape or dimensions of the junction. It is solely a function of the difference in the average entropies of the charge carriers in the two materials, and of the temperature of the junction.

The rate of reversible heat flow across a junction between two dissimilar conductors due to the Peltier effect is given by,

$$Q = \alpha_{AB} T I \quad \text{watts} \tag{2.6}$$

where Q is the heat flow, α_{AB} is the relative Seebeck coefficient of the two materials, T is the junction temperature in Kelvin, and I is the current flow across the junction. For simplicity, α_{AB} is assumed constant with temperature. The variables α and T can be combined into one term called the Peltier coefficient Π,

$$\Pi_{AB} = \alpha_{AB} T \quad \text{volts} \tag{2.7}$$

where Π_{AB} is the relative Peltier coefficient and is the difference of the absolute Peltier coefficients of the two conductors. By convention, Π_{AB} is taken as positive when heat is

absorbed at the junction through which current flows from conductor A to conductor B.

This necessary interchange in energy is illustrated in Figure 2.4 for an ideal junction between a metal and an n-type semiconductor [17]. Let us assume that an electric current is crossing the junction as indicated. In the semiconductor, the average energy of the moving electrons referenced to the Fermi energy E_F is ΔE_t. Similarly, in the metal, the average energy of the transported electrons referenced to the Fermi energy is ΔE_m. Therefore, when electrons cross from the metal into the semiconductor they must absorb energy equal to $\Delta E_t - \Delta E_m$. Generally ΔE_m is small compared to ΔE_t and so the energy absorbed by the electrons can be approximated by ΔE_t. The absorption of energy by electrons crossing from the metal to the n-type semiconductor results in a decrease in the junction temperature. It can be clearly seen that if the direction of current flow was reversed, heat would be released at the junction and so it will increase in temperature.

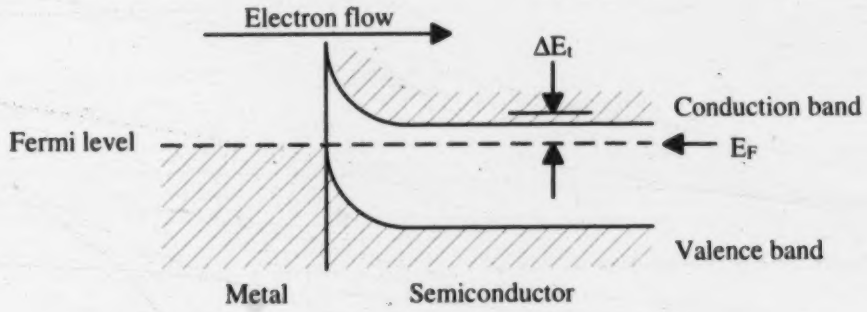

Figure 2.4: Energy band diagram of a metal-n-type semiconductor junction.

In a p-type semiconductor, the energy of the holes is less than the Fermi energy. When electrons flow from the metal into the semiconductor, the electrons recombine with holes in the semiconductor's valence band, releasing energy which results in an increase in the junction temperature. The Peltier effect is opposite for metal-p-type semiconductor junctions, than for metal-n-type semiconductor junctions.

In the non-ideal metal-semiconductor junction, electrons crossing the junction may encounter a barrier potential at the junction. This potential could be due to an applied bias voltage across the junction, trapped charges at the junction, the presence of dangling bonds, or an image force seen by charge carriers in close proximity to the metal. The non-equilibrium junction barrier potential results in a discontinuity in the Fermi energy at the junction, and so electrons crossing the junction will suffer a further change in energy. However, the energy gained or lost will be due to the barrier potential, and not due to an interchange in thermal energy (heat) with the surroundings. Hence, the barrier potential is not considered in the Peltier effect.

2.2.4 The Thomson Effect

In 1854 W. Thomson (Lord Kelvin) showed that heat is liberated or absorbed when an electric current flows in the same or opposite direction as the flow of heat in a conductor. He discovered this effect while trying to explain discrepancies between experimental results and his derived relationship between the relative Seebeck and Peltier coefficients.

The Thomson effect is illustrated in Figure 2.5. Consider a single uniform conductor in which points A and B are initially at a temperature T_1, and which is heated at some point O to a temperature T_2 ($T_2 > T_1$). The electrons flowing past A toward O will absorb energy in moving against the temperature gradient.[1] Their potential energy increases and so the net heat outflow from point O to A decreases. Similarly, electrons flowing past O toward B will give off energy in moving with the temperature gradient. The net heat outflow from point O to B then increases. The net result being that point A will decrease in temperature and point B will increase in temperature. Consequently, it can be said that

[1] This energy absorption is easily understood when one considers that conducting electrons undergo scattering collisions with the conductor lattice during their travel. This results in an interchange of energy with the lattice. In a good conductor the average distance of travel, the mean free path, of electrons is quite small (406 Å at 0 °C for gold [18] is typical for good conductors). Therefore, electrons undergo a great many collisions with the conductor lattice.

heat is absorbed at A and liberated at B. Due to the uniform nature of the conductor, the temperatures at A and B will equally differ from T_1 by an amount ΔT, and point O will remain at a constant temperature T_2. The Thomson effect is present only when a current flows in a conductor in a temperature gradient.

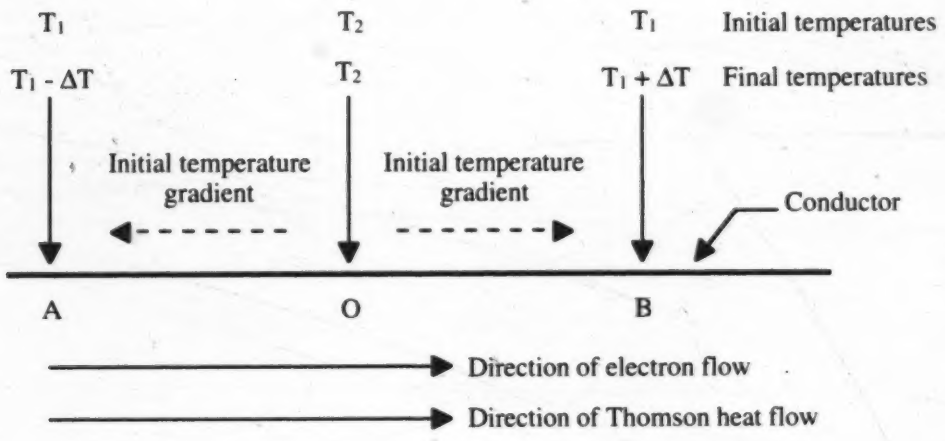

Figure 2.5: The Thomson effect.

The Thomson coefficient (τ) is the change in the heat content within a single conductor of unit cross section when a unit quantity of electricity flows through it through a temperature gradient of 1 K. It has the units volts/K. It is sometimes called the specific heat of electricity. $\tau > 0$ implies that heat is absorbed when the current flows toward regions of higher temperature. The heat flow due to the Thomson effect is given by,

$$Q = \tau I \frac{dT}{dx} \quad \text{watts} \qquad (2.8)$$

where Q is the heat flow, I is the electric current flow in the conductor, and T is the temperature in Kelvin.

The three thermoelectric effects are related by the Kelvin relationships shown in Equations (2.9) and (2.10). In these equations the subscript A refers to the conductor under investigation.

$$\alpha_A = \frac{\Pi_A}{T} \tag{2.9}$$

$$\frac{\tau_A}{T} = \frac{d\alpha_A}{dt} \tag{2.10}$$

Equation (2.10) can be integrated to give Equation (2.11) to calculate the absolute Seebeck coefficient of a conductor as a function of temperature.

$$\alpha_A(T) = \int_0^T \frac{\tau_A(t)}{t}\, dt \tag{2.11}$$

where $\alpha_A(0) = 0$ has been invoked. By using Equation (2.11), $\alpha_A(T)$ can be determined from measurements on a single conductor. In practice, accurate measurements of $\tau_A(t)$ are very difficult to make. Therefore, they have been carried out for only a few metals, most thoroughly for lead. Lead is then typically used as a standard for determining $\alpha_A(T)$, by using measurements of $\alpha_{AB}(T)$ in conjunction with Equation (2.5).

The Thomson effect is not of primary importance in thermoelectric devices as its effect is small, and can be neglected in non-detailed calculations [19].

2.3 Thermal Conductivity In Solids

Thermal conductivity in solids is highly dependent on temperature and the atomic structure of the material. Thermal conduction (κ) within a solid can be written as the sum of two components; conduction by charge carriers (κ_e), and conduction by lattice waves (κ_L).

$$\kappa = \kappa_e + \kappa_L \tag{2.12}$$

The magnitudes of both these components of thermal conduction are temperature dependent. Their variation with temperature will not be discussed here as it is beyond the scope of this thesis.

At room temperature, thermal conduction by charge carriers is dominant in metals, while conduction by lattice waves is dominant in electrical insulators. In semiconductors, the lattice thermal conductivity is generally independent of the carrier concentration and is the dominant effect in moderately doped semiconductors (typically < 10^{18} atoms/cm^{-3}) [20]. Figure 2.6 shows the variation in the thermal conductivity of Bi_2Te_3 as a function of temperature, illustrating the component of the thermal conductivity due to lattice waves.

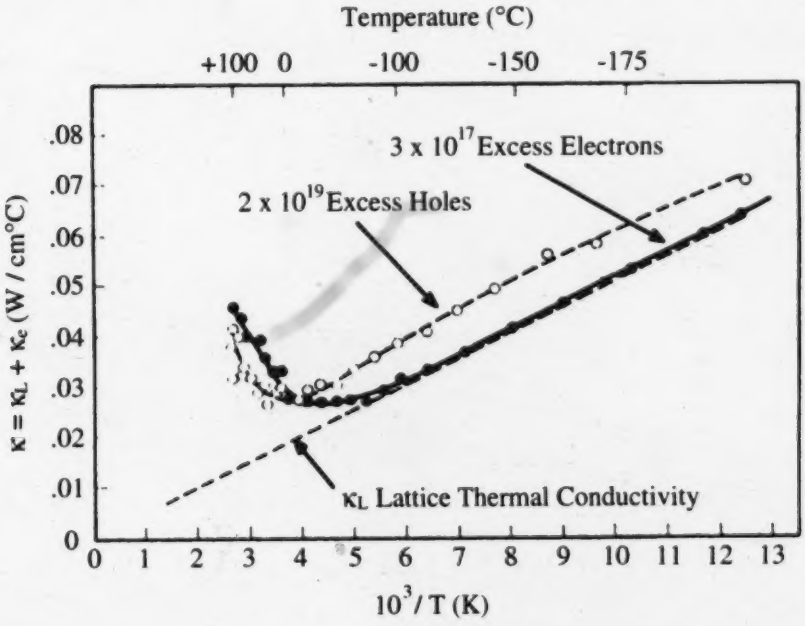

Figure 2.6: The thermal conductivity of Bi_2Te_3 as a function of temperature. The component of the thermal conductivity due to lattice waves is indicated by the dashed line [17].

2.3.1 Thermal Conduction By Lattice Waves

In lattice thermal conduction (κ_L), thermal energy is transported by lattice vibrations. The energy of these vibrations is quantized into an integral number of phonons, each possessing a momentum and an energy hν (where h is Plank's constant, and ν is the frequency of oscillation of the lattice wave). At thermal equilibrium, the phonons in a solid are isotropically distributed in momentum space [21]. When a temperature gradient is present, the phonon distribution is asymmetrical. An interchange of energy among the lattice waves takes place, which tends to restore equilibrium.

The rate at which equilibrium is restored is associated with the mean free path between collisions for the phonons. The greater the mean free path, the greater the phonon thermal conduction. The mean free path is the average distance a phonon will travel before undergoing a collision. This collision can be with another phonon or with atoms in the crystal lattice. At low temperatures, scattering by atoms in the crystal lattice tends to be dominant, while at higher temperatures phonon-phonon scattering is usually dominant. Phonons can also be scattered by free charge carriers in a solid. Consequently, the lattice thermal conductivity is reduced in metallic conductors due to their high carrier concentration [22].

Scattering by atoms in the crystal lattice is highly dependent on defects in the lattice, such as impurities, grain boundaries, or dislocations. Accordingly, amorphous materials, glasses, and polycrystalline materials generally possess a smaller thermal conductivity than single crystals of the same materials. Defects are often purposefully introduced in materials in an attempt to reduce their thermal conductivity.

Disorder may also be introduced by alloying materials. If the atoms involved have different masses but are chemically similar, then the resultant alloy will possess similar electronic properties, but the lattice thermal conductivity may be as much as 10 times lower [20]. Figure 2.7 is a plot of the thermal resistivity of various germanium-silicon alloys. In the central range of composition, the thermal resistivity is increased greatly from that of pure germanium and silicon.

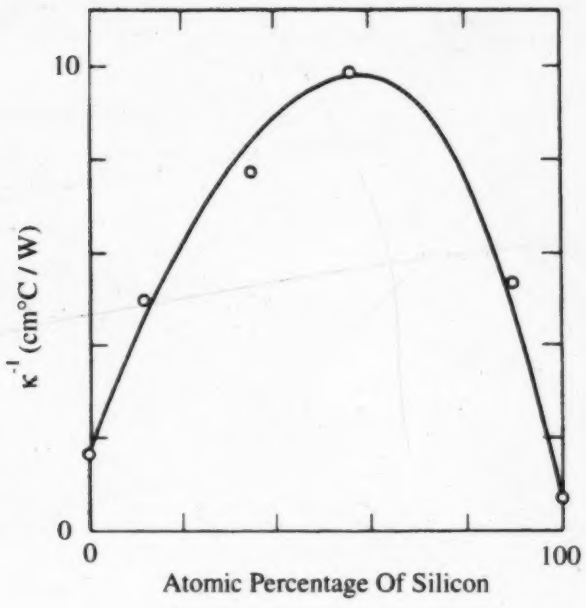

Figure 2.7: Thermal resistivity at 300 K as a function of composition in the Ge-Si system [17].

Compound semiconductors can also possess reduced lattice thermal conductivity. At room temperature, the wavelengths of the thermal conduction phonons are of the order of a few interatomic spacings [22]. Thus, conduction phonons are readily scattered in compound semiconductors, as scattering is most effective over quarter wavelength disturbances in periodicity.

Materials made up of heavy atoms generally have low lattice thermal conductivities [17,20]. For this reason, compound semiconductors such as bismuth telluride and lead telluride are useful thermoelectric materials due to their low thermal conductivities. Table 2.1 lists lattice thermal conductivities for various semiconductors at room temperature. The reliability of some of the data in this table is questioned by its author [22], and references are included in the original text.

Table 2.1: Lattice thermal conductivity of semiconductors at room temperature [22].

Semiconductor	Groups	κ_L (W/cm°C)
Diamond	IV	5.5
Si	IV	1.45
Ge	IV	0.64
GaAs	III-V	0.37
Te	VI	0.03
PbTe	IV-VI	0.023
Sb_2Te_3	V-VI	0.024
Bi_2Te_3	V-VI	0.016

2.3.2 Thermal Conduction By Charge Carriers

In thermal conduction by charge carriers (κ_e), thermal energy is transported via the kinetic energy of electrons carrying electric current. Accordingly, electron thermal conduction is related to the electrical conductivity of a material, and so to the number of charge carriers and their mean free path. Scattering mechanisms, such as those discussed for phonon travel in solids in section 2.4.1, also play a part in electron thermal conduction.

Figure 2.8 shows the room temperature thermal conductivity of Bi_2Te_3 plotted against its electrical conductivity. The thermal conductivity is seen to increase with electrical conductivity for $\sigma > 0.5 \times 10^3\ \Omega^{-1}cm^{-1}$.

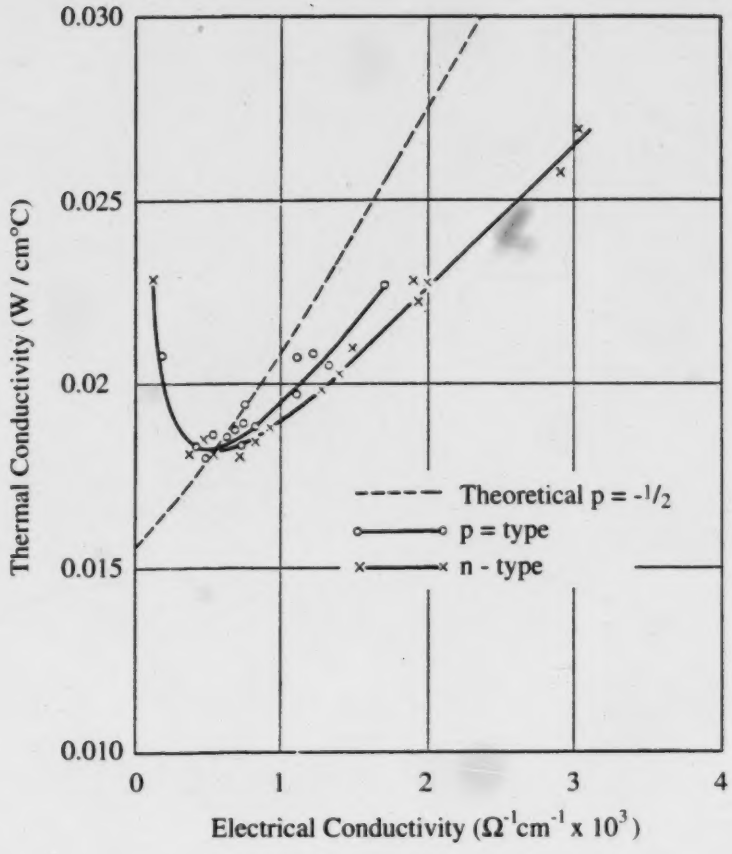

Figure 2.8: Thermal vs. electrical conductivity for of Bi_2Te_3 at 300 K [22].

2.4 A Peltier Heat Pump

The following discussion will use several simplifying assumptions. The problem of heat transfer to the surroundings (air or other media) will not be considered. It will be assumed that the electrical resistance at junctions between conducting materials is negligible compared to the bulk resistance of the materials. In addition, the electrical resistivity (ρ), thermal conductivity (κ), and Seebeck coefficients (α) of all materials are assumed independent of temperature. The assumption of a thermally independent Seebeck coefficient

results in a Thomson coefficient of zero by Equation (2.10), and so the Thomson effect can be neglected.

Figure 2.9 shows a schematic of a two-junction Peltier heat pump comprised of two conductors A and B. Junction 2 is set in a thermal reservoir at a constant temperature T_1. Junction 1 is in a second thermal reservoir at a temperature $T_1 - \Delta T$, where ΔT is set by the Peltier heat pump. The net heat which is absorbed or given off at each junction of the Peltier pump is the sum of three terms; the Peltier heat at the junction, Joule heating generated in the conducting materials due to current flow, and heat flow through the conducting materials via thermal conductivity.

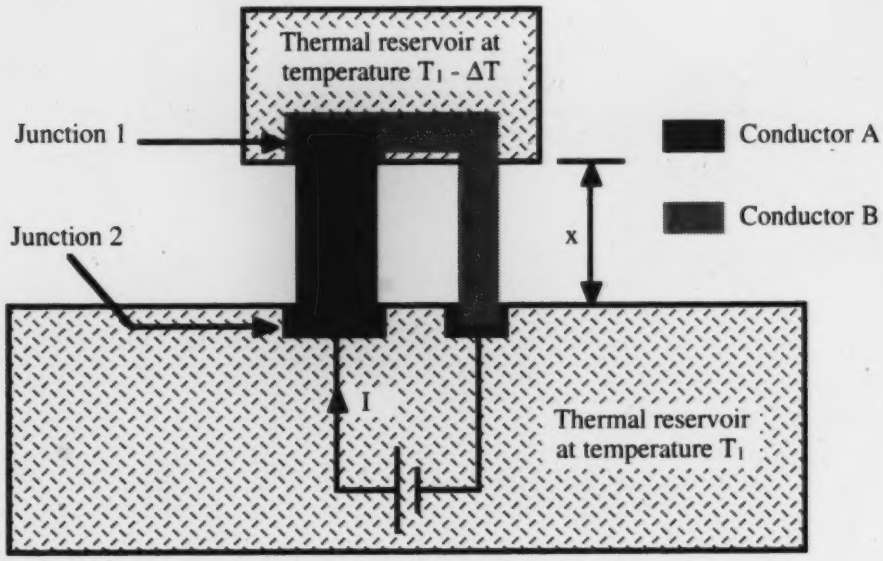

Figure 2.9: Schematic of a two-junction Peltier device.

Consider the situation at junction 1. The Peltier heat at junction 1 is given by Equation (2.6), which is expanded below for the device of Figure 2.9.

$$Q_P = \alpha_{AB} (T_1 - \Delta T) I \quad \text{watts} \tag{2.13}$$

The Joule heating generated in conductors A and B will flow both towards junction 1 and junction 2. Under the assumption that the thermal conductivity of conductors A and B is independent of temperature, one half of the Joule heating will flow toward each junction.[2] Thus, for junction 1 the Joule heating is,

$$Q_J = {}^1/_2 (R_A + R_B) I^2 \quad \text{watts} \tag{2.14}$$

where R_A and R_B are the electrical resistances of conductors A and B respectively.

Heat flow between the two thermal reservoirs by means of thermal conduction through A and B is given by,

$$Q_T = \left(\frac{\kappa_A S_A}{L_A} + \frac{\kappa_B S_B}{L_B} \right) \Delta T \quad \text{watts} \tag{2.15}$$

where κ, S, and L are the thermal conductivity, cross-sectional area, and length of conductors A and B respectively, and ΔT is the temperature difference between the two thermal reservoirs. Under the assumption that the thermal reservoirs of Figure 2.9 are ideal, L_A and L_B would be equal to the distance x separating the reservoirs.

Summing Equations 2.13 to 2.15, the net heat pumped at junction 1 of Figure 2.9 is,

$$Q = \alpha_{AB}(T_1 - \Delta T)I - {}^1/_2 (R_A + R_B)I^2 - \left(\frac{\kappa_A S_A}{L_A} + \frac{\kappa_B S_B}{L_B} \right) \Delta T \quad \text{watts} \tag{2.16}$$

or

$$Q = \alpha_{AB} T I - {}^1/_2 R I^2 - K \Delta T \quad \text{watts} \tag{2.17}$$

where T is the junction temperature $(T_1 - \Delta T)$, R is the total electrical resistivity

---

[2] The error due to this assumption is not significant for the small temperature differential produced by the micro-Peltier device.

$(R_A + R_B)$, and K is the total thermal conductivity $\left(\frac{\kappa_A S_A}{L_A} + \frac{\kappa_B S_B}{L_B}\right)$. Using the sign convention stated for the Peltier coefficient in Equation 2.7, the heat pumping rate is taken as positive when heat is absorbed at a junction. Thus, Joule heating and thermal conduction in Equations 2.16 and 2.17 are negative, and Q accordingly indicates the rate of heat removal.

When operating in the cooling mode, the electric current (I) at which the maximum heat pumping rate occurs is obtained by differentiating Equation 2.17 with respect to I and setting the derivative equal to zero. Solving for I we obtain,

$$I = \frac{\alpha_{AB} T_{Cold}}{R} \quad \text{amps} \tag{2.18}$$

Substituting Equation 2.18 into 2.17, the maximum cooling rate is,

$$Q_{max} = \frac{(\alpha_{AB} T_{Cold})^2}{2R} - K\Delta T \quad \text{watts} \tag{2.19}$$

2.5 Selection Of Materials For A Peltier Heat Pump

Equation 2.17 indicates that an efficient Peltier heat pump should be fabricated from materials which together possess a high relative Seebeck coefficient (α_{AB}), low electrical resistivity, and low thermal conductivity. All three of these quantities are a function of the density of free charge carriers. This is shown in Figure 2.10 (a). It is seen that the electrical conductivity increases with carrier concentration. The absolute Seebeck coefficient is large for small carrier concentrations (electrical insulators and semiconductors), and is small for large carrier concentrations (metals). The thermal conductivity is seen to increase with electrical conductivity.

Selecting materials which favorably possess all the above quantities is a non-trivial one. Materials with low electrical resistivity (typically metals) generally possess a high thermal conductivity and a low absolute Seebeck coefficient. Poor thermal conductors (woods, rock minerals, glasses) are generally electrical insulators. Semiconductors possess

a wide variation of the above quantities depending on their doping and material composition. A way of evaluating a given material for use in a Peltier pump is to determine its figure of merit.

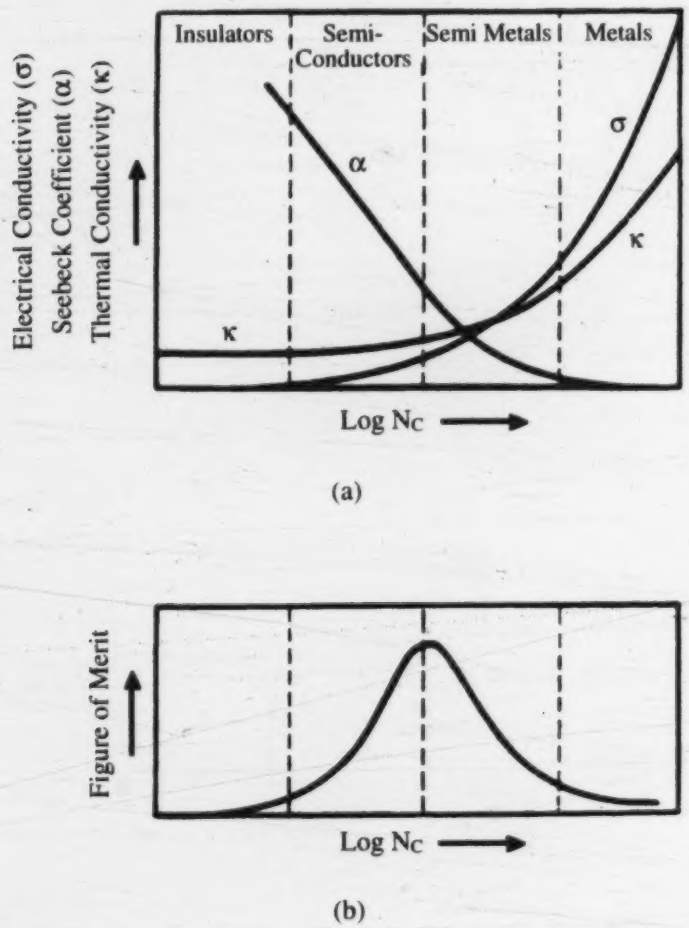

Figure 2.10: Schematic showing the properties of materials as a function of electron concentration N_C [17].

2.5.1 Figure Of Merit

The coefficient of performance, or figure of merit (z), is used to evaluate the efficiency of a thermoelectric material when used as a Peltier heat pump. When selecting appropriate thermoelectric materials for a Peltier device, materials are selected on the basis of maximizing their figure of merit over the operational temperature range. For a single material, the figure of merit is given by [7,17],

$$z = \frac{\alpha^2}{\rho\kappa} \quad K^{-1} \tag{2.20}$$

where α is the absolute Seebeck coefficient, ρ is the electrical resistivity, and κ is the thermal conductivity of the material.

Figure 2.10 (b) shows the figure of merit of materials as a function of electron concentration. From this figure it appears that semiconductors are favorable thermoelectric materials for use in Peltier heat pumps. Selection of charge carrier doping for the semiconductor is critical as both the Seebeck coefficient and electrical conductivity vary with doping. The conductivity increases with increasing doping, while the Seebeck coefficient decreases. The figure of merit reaches a maximum at some intermediate density of doping, typically 10^{19} atoms/cm^{-3} [20]. Table 2.2 lists the figure of merit of various materials. Metals listed in Table 2.2 are those in common use in the semiconductor industry and at the Alberta Microelectronic Centre.

Table 2.2: Figure of merit of various semiconductors and semi-metals.

Material	α (μV / °C)	ρ (μΩcm)	κ (W / cm°C)	z ($x10^{-3}$ K^{-1})	Temp. (K)	Ref.
Semi-metals						
88% Bi + 12% Sb				6.0	80	[20]
Semiconductors						
Si, n-type	450	3500		0.04	room	[11]
SiGe, n-type				0.9	900	[20]
PbTe, n-type				1.9	500	[20]
PbTe, p-type				1.8	600	[20]
Bi_2Te_3, n-type	-200	790	0.019	2.7	room	[6]
Bi_2Te_3, p-type	210	1090	0.018	2.2	room	[6]
Sb_2Te_3, p-type	130	500	0.028	1.2	room	[7]
90% Bi_2Te_3 + 5% Sb_2Te_3 + 5% Sb_2Se_3, n-type				3.2	300	[20]
Metals[3]						
Al	-1.7	2.655	2.37	0.00046	room	[7]
Au	1.94	2.35	3.15	0.00051	room	[7]
Cr	17.3	13	0.91	0.025	room	[7]
Mo	5.57	5.2	1.4	0.0043	room	[7]
W	1.07	5.65	1.78	0.00011	room	[7]
Sb	40	41.8	0.185	0.21	room	[17]
Bi	-60	115	0.084	0.37	room	[17]

[3] The reference provided in the table for the these materials applies to the Seebeck coefficient only. Numerical values for ρ and κ were obtained from [80].

2.5.2 Figure Of Merit For Peltier Devices

A two-junction Peltier heat pump (see Figure 2.9) is comprised of two different thermoelectric materials. For such a device, the figure of merit must be calculated for both materials. Using Equation 2.20 (the figure of merit for a single material) as a starting point, we see that the numerator is the square of the absolute Seebeck coefficient of the material, and the denominator is the product of its resistivity and thermal conductivity. For a couple (two thermoelectric materials forming a junction) the relative Seebeck coefficient α_{AB} (where A and B are the two materials making up the couple) can be used. The situation for the denominator is, however, more complicated.

For a single material, its resistance and thermal conductance are found from,

$$R = \frac{\rho L}{A} \quad \Omega \tag{2.21}$$

$$K = \frac{\kappa A}{L} \quad W / cm\,K \tag{2.22}$$

where R is the resistance of the material, K is its thermal conductance, L is its length, and A is its cross-sectional area. R and K can be used in place of ρ and κ in Equation 2.20, since the R and K for a given material are determined from its length and cross-sectional area with opposite ratios.

For a couple (looking from the thermal reservoir at temperature T_1 - ΔT in Figure 2.9 toward the reservoir T_1) we can denote R and K to be,

$$R = \rho_A/\gamma_A + \rho_B/\gamma_B \quad \Omega \tag{2.23}$$

$$K = \kappa_A/\gamma_A + \kappa_B/\gamma_B \quad W / cm\,K \tag{2.24}$$

where R is the resistance of materials A and B in series, K is the thermal conductance of A and B in parallel, and γ_A and γ_B are the ratio of cross-sectional area to length for A and B. The product of RK is,

$$RK = \kappa_A\rho_A + \kappa_A\rho_B(\gamma_A/\gamma_B) + \kappa_B\rho_A(\gamma_B/\gamma_A) + \kappa_B\rho_B \qquad (2.25)$$

The figure of merit for the couple is found by substituting RK and α_{AB} into Equation 2.20. Thus,

$$z_{AB} = \frac{\alpha_{AB}^2}{RK} \quad K^{-1} \qquad (2.26)$$

or

$$z_{AB} = \frac{\alpha_{AB}^2}{\kappa_A\rho_A + \kappa_A\rho_B(\gamma_A/\gamma_B) + \kappa_B\rho_A(\gamma_B/\gamma_A) + \kappa_B\rho_B} \quad K^{-1} \qquad (2.27)$$

z_{AB} can be maximized by minimizing RK. This is done by selecting material dimensions for A and B to optimize γ_A and γ_B (Thus, minimizing Joule heating and thermal conductivity losses.). RK_{min} is found by differentiating Equation 2.25 by γ_A/γ_B and setting the partial derivative to zero. Thus,

$$\gamma_A/\gamma_B = \left(\kappa_B\rho_A / \kappa_A\rho_B\right)^{1/2} \qquad (2.28)$$

Substituting into Equation 2.25, we obtain,

$$RK_{min} = \left(\left(\rho_A\kappa_A\right)^{1/2} + \left(\rho_B\kappa_B\right)^{1/2}\right)^2 \qquad (2.29)$$

Substituting into Equation 2.26 we obtain,

$$z_{AB\,max} = \frac{\alpha_{AB}^2}{\left(\left(\rho_A\kappa_A\right)^{1/2} + \left(\rho_B\kappa_B\right)^{1/2}\right)^2} \quad K^{-1} \qquad (2.30)$$

2.5.3 Maximum Temperature Difference

The maximum temperature differential that can be achieved between the hot and cold sides of a two-junction Peltier device is found by solving for ΔT in Equation 2.19 with Q_{max} set to zero (There is no net heat pumping at the maximum temperature difference.).

Thus,

$$\Delta T = \frac{(\alpha_{AB} T_{Cold})^2}{2RK} \quad K \tag{2.31}$$

or

$$\Delta T_{max} = \tfrac{1}{2} z_{AB} T_{Cold}^2 \quad K \tag{2.32}$$

using Equation 2.26. Equation 2.32 shows that the greater the value of z_{AB}, the greater the temperature reduction possible.

The maximum possible temperature differential achievable by a two-junction Peltier device is found by substituting $z_{AB\,max}$ in Equation 2.32. Thus,

$$\Delta T_{max} = \tfrac{1}{2} z_{AB\,max} T_{Cold}^2 \quad K \tag{2.33}$$

2.5.4 Figure Of Merit vs. Maximum Cooling Ability

Equation 2.19 yields the maximum cooling rate of a Peltier device at a temperature difference of ΔT. At zero temperature difference ($\Delta T = 0$), Equation 2.19 reduces to,

$$Q_{max_0} = \frac{(\alpha_{AB} T_{Cold})^2}{2R} \quad \text{watts} \tag{2.34}$$

There are two performance benchmarks for a Peltier device; Q_{max_0} and figure of merit (Equation 2.26). Which equation one selects when optimizing the design of a Peltier device depends on the application for the Peltier device.

Q_{max_0}, unlike the figure of merit, does not take into account the thermal conductivity of the materials comprising the Peltier device. Therefore, if one were only interested in achieving a high cooling power one would use Equation 2.34, and so materials possessing a high ratio between relative Seebeck coefficient and electrical resistivity should be considered.

If one were constructing an efficient Peltier device, that is to say a device which

uses the minimum amount of power to maintain a constant temperature difference, the figure of merit should be used to evaluate selected materials.

For the micro-Peltier pump high efficiency was desired. Therefore, the figure of merit was the selection criteria for materials in its construction. Material selection for the micro-Peltier pump is discussed in sections 3.4 and 3.5.

2.6 Other Methods Of Heat Transfer

In addition to thermal conduction, convection and radiation are also methods of thermal energy transfer. They are discussed briefly below.

2.6.1 Thermal Convection

Thermal convection is the transfer of heat by the mixing of molecules of a fluid (or gas) with the bulk fluid after thermal energy has been exchanged with a hot or cold surface (This exchange is by thermal conduction.). The motion of the fluid (or gas) to bring about mixing is due to differences in density. Convection models will not be discussed for the micro-Peltier pump, because its maximum performance testing was conducted in a vacuum environment.

2.6.2 Thermal Radiation

Thermal radiation is due to the emission of photons from a surface. The net energy transferred from a surface due to thermal radiation is equal to the difference between the radiation emitted from the surface under study and absorbed from the surrounding surfaces. It is given by,

$$Q_r = \varepsilon\sigma\left(T_s^4 - T_o^4\right) \quad W/m^2 \qquad (2.35)$$

where T_S is the temperature of the surface in Kelvin, T_O is the temperature of the surroundings, ε is the emissivity of the surface, and σ is the Stefan-Boltzmann constant. Losses due to thermal radiation are discussed in section 4.3.4.

Chapter 3

FABRICATION OF THE MICRO-PELTIER PUMP

"If at first you don't succeed, try again. Then quit. No use being a damn fool about it."

-- W. C. Fields

3.1 Introduction

The various material components of the Peltier pump were described in section 1.4. This chapter discusses in some detail the selection criteria for these materials, and how they are integrated into the fabrication of the Peltier pump. These latter discussions include details on material deposition, photolithographic masking, and patterning using various etchants. It is assumed that the reader possesses knowledge of the basic concepts of thin film deposition (thermal evaporation and sputtering), photolithography, and chemical etching of thin films (both wet and dry etching).

Several fabrication and processing problems had to be solved during this thesis and these issues were often unrelated to each other. A brief outline to the various sections of this chapter is given below to help coordinate the discussions of this chapter.

- Section 3.2 discusses the use of linotronic printed masks as a lower cost alternative to standard photolithographic masks.

- Section 3.3 considers the thermal isolation of the micro-Peltier pump. Thin film stress issues and decisions leading to the selection of a SiO_2 microbridge are presented.

- The selection criteria for the materials used in the construction of the Peltier device (Bi_2Te_3 and gold) are explained in section 3.4.

- In section 3.5, the decision to use gold metal over aluminum metal is explained. Adhesion problems with gold are also touched on.

- Section 3.6 presents Bi_2Te_3 processing details. Discussions cover its properties, deposition, substrate temperature, uniformity, and oxygen impurities.

- The lengthy processing steps used in the fabrication of the Peltier device are presented in section 3.7.

- Section 3.8 details processing issues. Discussions cover the adhesion of Bi_2Te_3, its etching, gold and adhesion metal etching concerns, gold diffusion and resistivity, and problems when freeing the SiO_2 microbridge.

- The last section of this chapter, section 3.9, discusses the passivation of the Peltier device with a SiO_2 thin film.

3.2 Linotronic Printed Photolithographic Masks

The micro-Peltier device requires six photolithographic masking steps for its fabrication. At $400-500 each, traditional pattern generation masks[1] were deemed too expensive for this thesis, especially considering the iterations necessary in building device

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[1] Standard photolithographic masks (chrome on glass) can be fabricated using pattern generation (light exposure of photoresist under a variable aperture) and by electron beam (E-beam) exposure of a resist. The pattern generation process is less precise (approximately 2 μm resolution) and less expensive than E-beam, but possesses sufficient resolution for the fabrication of the micro-Peltier device. Pattern generation masks used by the Alberta Microelectronic Centre have been purchased from PPM Photomask Inc. at a cost of around $400-500 each.

prototypes. Linotronic printed masks were selected as a lower cost alternative. One 8.5 x 11 inch linotronic printing can hold six 3 inch mask designs and costs $36 to print with a 24 hour turn around time. This is a significant cost and time saving over conventional mask generation.

3.2.1 Linotronic Masks - Fabrication And Usage

Mask designs are made using the software L-Edit™ purchased from Tanner Research Inc.. These designs are saved in PostScript format and submitted for linotronic printing to Contempratype Typographers Ltd., Edmonton, Alberta. Linotronic printing is done at 3386 dpi (7.50 μm) resolution onto transparent photographic film sheets. These sheets are cut to size and then fixed onto 4" mask glass plates which enables their mounting in the photolithographic mask aligner. Due to the non-ideal transmission properties of the photographic film sheets, UV exposure times are increased by a factor of ~ 1.5 when exposing photoresist through these masks.

3.2.2 Linotronic Masks - Design Rules

The dimensional fidelity of PostScript generated masks is of key concern. There are several factors which can affect the quality of the mask. Some are, the quality of the ink used, the condition of the linotronic printer, and which part of the roll of linotronic film sheet the mask is printed on. The middle of the roll tends to suffer less stretch during printing than the ends, and so it has higher resolution accuracy. Good linotronic print shops keep the middle of rolls in storage for when a high quality printing is demanded. The software program on which the mask is rendered is also of importance. Many software packages do not render PostScript with true dimensional accuracy. These packages prefer instead to use the accuracy dictated by their internal ruler scaling governing

printing[2] or by the printer driver selected. Just because the on screen ruler is set to microns in the CAD or drawing package used, it does not mean that the PostScript generated file will use these ruler settings. These factors and more bring into question the dimensional fidelity and repeatability of PostScript generated masks. A good discussion of PostScript mask generation and problems is given in [23].

The main problem with linotronic printing is the scattering and flowing of the deposited ink particles at feature edges. Feature edges are rough and poorly defined for up to 5 μm in from the edge. Features are also often wider than expected as the linotronic ink will travel beyond the desired feature edge. Typical distance of ink travel is about 1-2 μm. Consequently, widths and spacings of features will differ from the original design. After etching, however, patterned features possess edges which are smoother than the original linotronic mask. This is due in part to over exposure and over developing in the photolithography step, and to some degree of "polishing" during the etching of the patterned thin film making up a feature. The amount of polishing varies with the level of undercut of the thin film during etch.

The poor feature resolution and repeatability of a linotronic image necessitates some forethought when fabricating linotronic masks. Several test masks were fabricated in order to gain some understanding of the required "design rules" when making linotronic masks. These rules are listed below.

- The maximum resolution of the linotronic printer is 3386 dpi or 7.50 μm. In order to avoid fractional round-off error, features sizes and spacings in the mask design should be multiples of 7.5 μm.

- Features (lines) should be 30 μm or wider to avoid significantly non-uniform widths. 7.5 μm lines are very non-uniform and are often non-continuous. 15 μm lines can be fabricated with good continuity, but possess significant variation in their widths. See Figures 3.1 to 3.4. It should be noted that the apparent curvature

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[2] For example, some Macintosh applications describe their graphic output in PICT or PICT2 formats. These formats are limited to 72 dpi or 0.35 mm.

of these lines is due to the optics of the microscope camera used to take this picture and not due to the linotronic image.

- Feature spacings should be at least 30 µm (4 times the 7.5 µm printing resolution) in order for a good quality gap to appear between features. Spacings between features which are closely placed can be locally filled in by linotronic ink. 15 µm spacings are typically filled in. See Figures 3.1 and 3.2.

- Right angles on a feature are rounded off due to ink spreading. Thus, feature spacings close to an inside right angle corner should be at least 30 µm to prevent contact between adjacent features. Closed features (a hollow square) should possess no less than 30 x 30 µm hollow space, as smaller spaces are often filled in. See Figure 3.5.

It can be seen that the patterned aluminum lines of Figures 3.1 to 3.5 possess rough edges. Linotronic printed masks are acceptable for fabricating conducting metallization lines and gross features, but are not suitable for precise photolithography work. Nonetheless, the quality of these masks is sufficient for this thesis and so this technique of mask making was selected.

3.2.3 Other Methods Of Mask Making

Two other mask generation techniques were investigated in an attempt to improve upon the resolution of linotronic masks. These were photo-reduction of linotronic masks and the use of photographic slides as masks. Both these techniques were abandoned as they provided no improvement over linotronic masks. They are discussed in some detail in Appendix A.

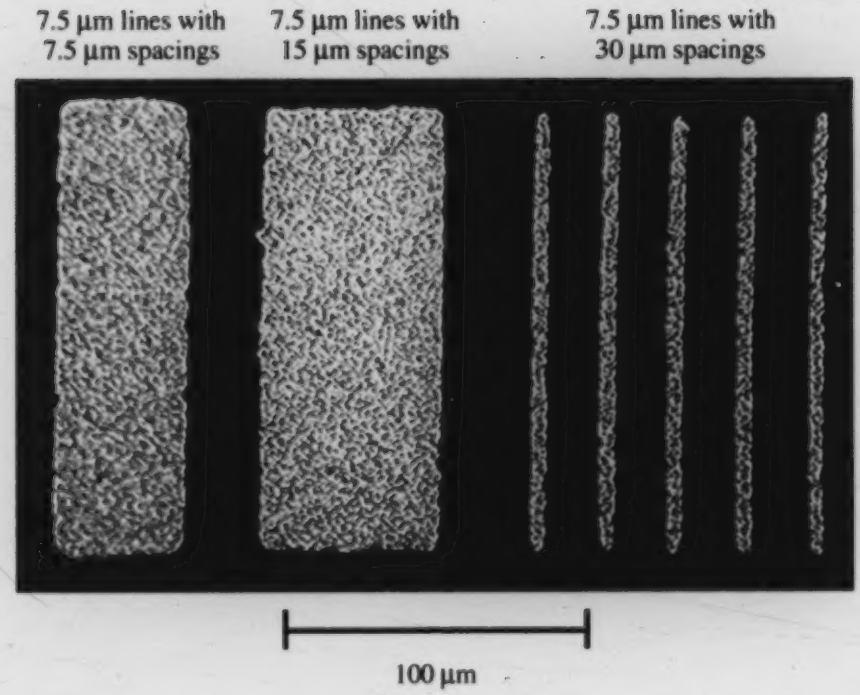

Figure 3.1: Lines patterned from 7.5 µm linotronic mask onto a 0.5 µm thick aluminum thin film. It can be seen that line spacings 15 µm or smaller are filled in. The line widths measure approximately 8.6 µm, an increase of 1.1 µm over the desired 7.5 µm line.

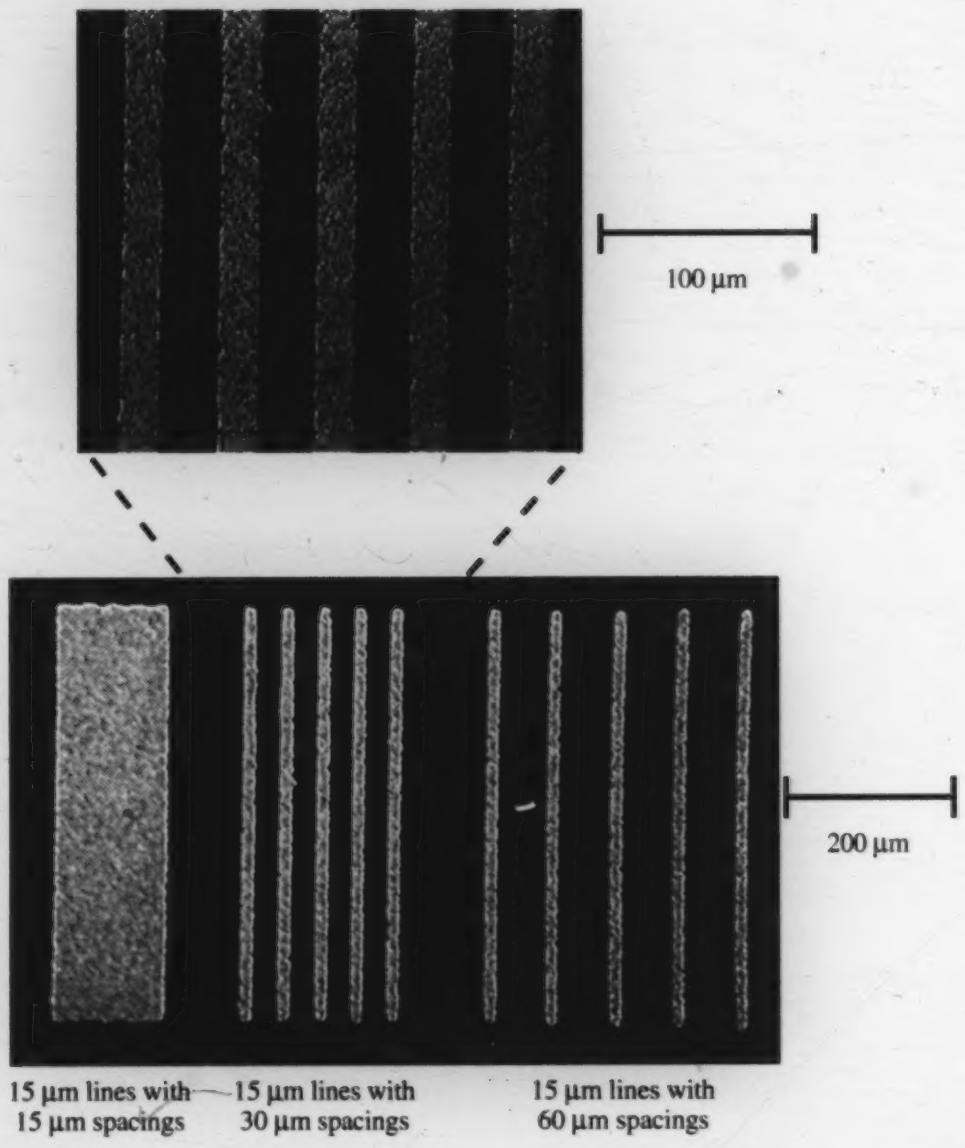

Figure 3.2: Lines patterned from 15 µm linotronic mask onto a 0.5 µm thick aluminum thin film. It can be seen that line spacings 15 µm or smaller are filled in. The line widths measure approximately 18 µm, an increase of 3 µm over the desired 15 µm line.

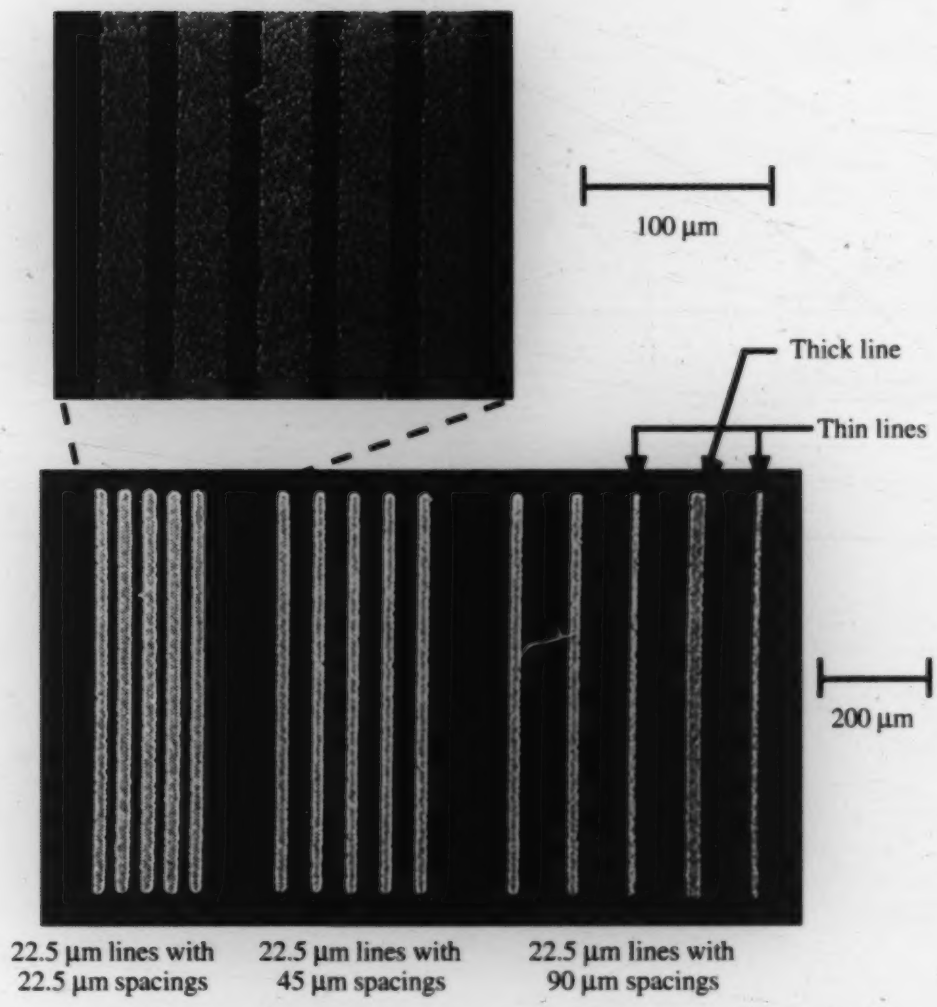
100 µm
Thick line
Thin lines
200 µm
22.5 µm lines with 22.5 µm spacings
22.5 µm lines with 45 µm spacings
22.5 µm lines with 90 µm spacings

Figure 3.3: Lines patterned from 22.5 µm linotronic mask onto a 0.5 µm thick aluminum thin film. It can be seen that the 22.5 µm line spacings are in danger of being filled in. The line widths measure approximately 25.5 µm, an increase of 3 µm over the desired 22.5 µm line. Some of the lines are thicker and thinner than the others (measuring approximately 33 and 17 µm in width respectively). These lines have been rounded off to larger and smaller sizes (linotronic line widths are integer multiples of 7.5 µm).

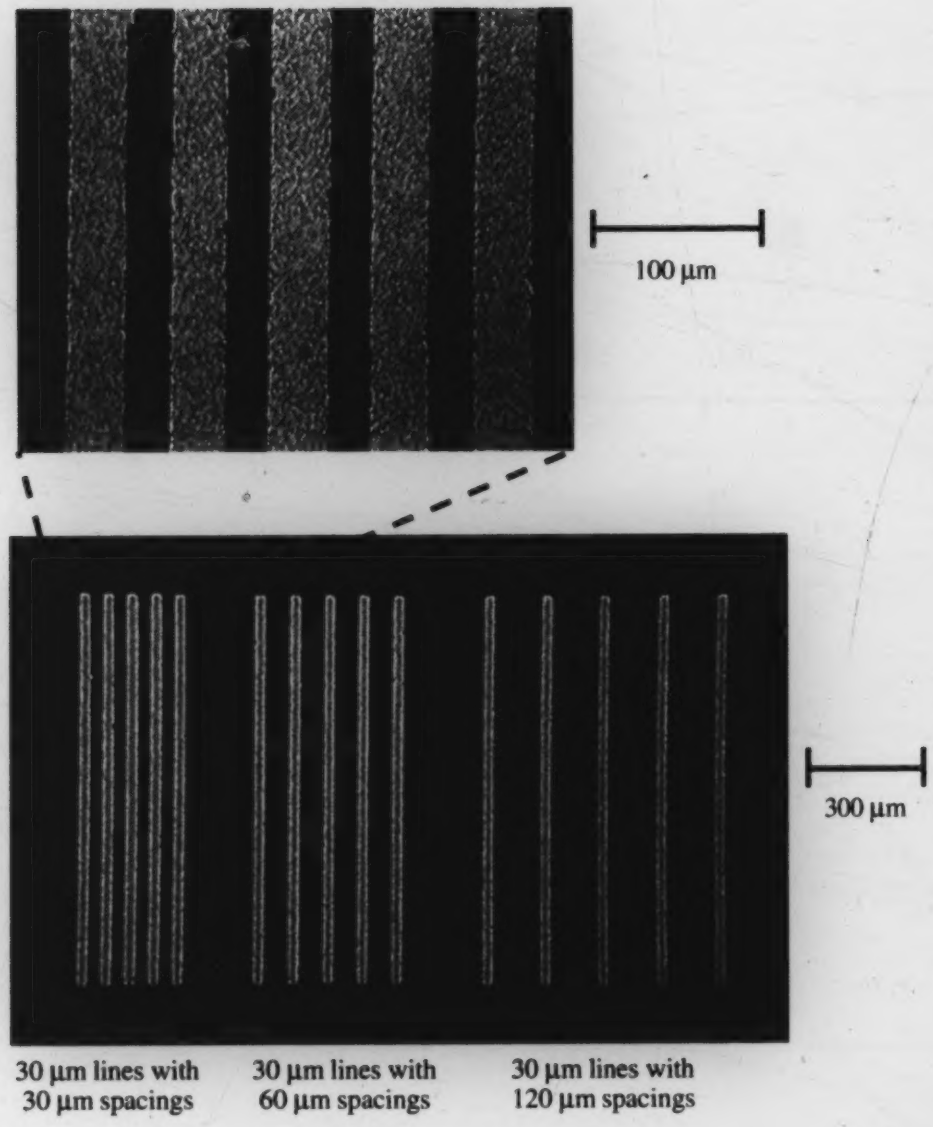

Figure 3.4: Lines patterned from 30 µm linotronic mask onto a 0.5 µm thick aluminum thin film. The line widths measure approximately 33 µm, an increase of 3 µm over the desired 30 µm line.

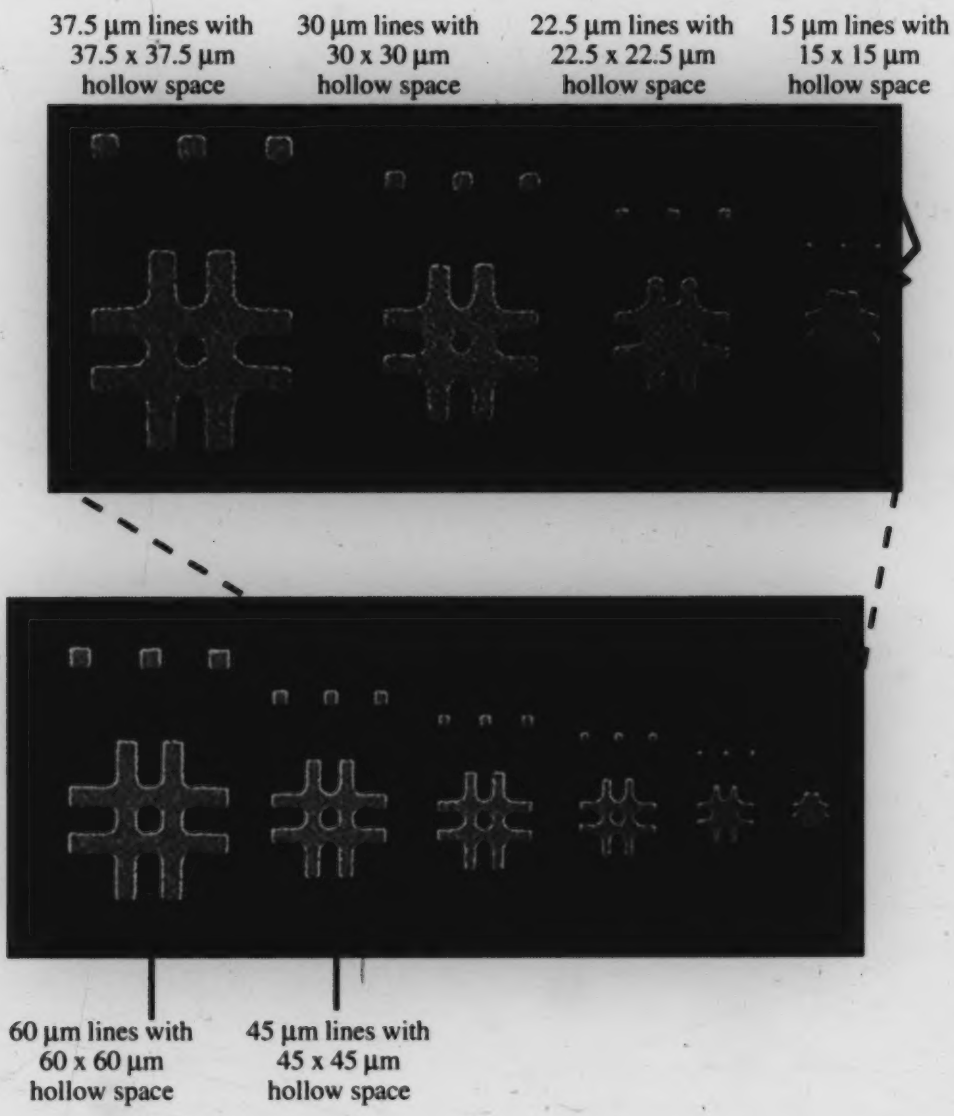

Figure 3.5: Right angled features are rounded off due to ink spreading. Closed features (hollow squares) should possess no less than 30 x 30 µm hollow space, as smaller spaces are often filled in.

3.3 Thermal Isolation Of The Micro-Peltier Device

Section 1.3 explained that the micro-Peltier pump is fabricated on a SiO_2 microbridge. The use of micro-fabricated structures (cantilevers, bridges, and diaphragms) for thermal load minimization is not a new idea. The low thermal and inertial mass of thin film microstructures has resulted in their use in a great many applications, from thermal isolation platforms [24-25], to highly sensitive integrated sensors [1-13,26] of all varieties. This thesis will not discuss the wide variety of micromachining techniques used in the fabrication of thin film microstructures. Only the techniques specifically used in the fabrication of the micro-Peltier pump are discussed. Those unfamiliar with silicon micromachining are directed to [27] which provides a good introduction to micromachining techniques.

3.3.1 Selection Of SiO_2 For The Microbridge

Thin films of silicon nitride (Si_3N_4), SiO_2, and SiO_2 - Si_3N_4 multi-layers are typically used in the fabrication of micromechanical structures, primarily due to their etch selectivity and low thermal and electrical conductivities.[3] For the micro-Peltier pump, the quality of the thermal isolation provided by the microstructure is of primary concern. Therefore, SiO_2 is used exclusively as the microbridge material since it has less than $^1/_{10}$ the thermal conductivity of Si_3N_4 (0.014 vs. 0.19 W/cm°C [28]).

3.3.2 Stress In Thin Film Microstructures

Of interest in the fabrication of microstructures is stress in the thin film(s) making up these structures. Significant stress can result in bending, buckling, or tension in the

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[3] Silicon dioxide has less than 1 % the thermal conductivity of silicon (0.014 vs. 1.57 W/cm-K [28]).

microstructure after it is released from the underlying silicon wafer. Extreme stress levels, those which exceed the critical stress for elastic deformation of the thin film microstructure, result in localized fracture and possible failure. These stress effects may also result in the separation or fracture of other thin film materials deposited on the microstructure.

Stress in a thin film has two components [29]. The first is stress inherent in the thin film itself (intrinsic or in-plane stress). This component is strongly dependent on the deposition technique and conditions during the deposition of the thin film. The second is differential stress characterized by the bending of the substrate-thin-film bi-layer due to differences in the thermal expansion coefficients of the substrate and thin film (thermal or bending stress). The vector direction of stress is characterized as being either compressive or tensile. Compressive stress is the desire of a thin film to want to expand outward from a point in a direction parallel to the substrate surface. Tensile stress is the desire to want to contract inward around a point in a direction parallel to the substrate surface.

Previous studies of thin film stress include stress variation with deposition technique [29] and reduction of stress by the annealing of already deposited films [26]. Another commonly used stress reduction technique is stress compensation by the deposition of variable stress SiO_2 - Si_3N_4 multi-layer structures [30]. This technique was not considered as Si_3N_4 is not used in the Peltier device. It should be mentioned that stress can also be introduced when freeing a microstructure from the underlying silicon wafer. This etch-induced stress was seen to cause failure of anisotropic etched cantilevers fabricated from stress relieved SiO_2 thin films for this thesis. A study was undertaken to understand the sources of this stress and how it can be avoided. Results of this investigation are presented in Appendix B.

3.3.3 Stress Relieved SiO_2 Films

In the fabrication of the micro-Peltier pump, PECVD SiO_2 deposited at 350 °C was chosen over thermally grown SiO_2 due to the lower stress levels in these films [29]. Films deposited by PECVD possess compressive stress. High temperature annealing

(1100 °C) in a nitrogen ambient for 20 minutes is used to reduce the stress in the SiO_2 films [26]. Films produced by this technique are sufficiently stress free to be used in the fabrication of the SiO_2 microbridge.

The annealing procedure is as follows. Wafers are loaded in the annealing oven at 800 °C. The oven is ramped up to 1100 °C, and upon arrival at this temperature the timer is started. After the desired time period, the oven heater is shut off, and the wafers are unloaded after cooling to 800 °C.

The annealing process affects the PECVD SiO_2 film by reducing trapped gases[4] and densifying the film. Also, the high annealing temperature results in some degree of "re-flow" of the oxide over the silicon substrate. This is because the thermal expansion coefficient of silicon is greater than that of SiO_2.[5] This leads to a lessening of the stress at the silicon-SiO_2 boundary. The result of this annealing process is that the stress in the SiO_2 thin film becomes less compressive. It can even become tensile in nature depending on how close the initial stress was to the compressive-tensile boundary.

3.3.4 SiO_2 Diaphragms - A Rejected Design

The fabrication of free standing microstructures requires the underlying silicon to be removed by etching. This posed a problem. The large dimensions of the Peltier device (100's of μm due to the resolution constraints of the linotronic masks) necessitated a silicon etch of several hours in length. This would require exposed areas of the Peltier device to be protected from the etchant. However, at the outset of this thesis, a method to passivate the Bi_2Te_3 was not available. The solution was to fabricate the SiO_2 thermal isolation platform first, and then to fabricate the micro-Peltier device on it. This resulted in the initial consideration of SiO_2 diaphragms for the thermal isolation platform. The SiO_2 diaphragms were to be fabricated by a backside etch technique. It was felt that their

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[4] Typically hydrogen is resident as SiH_4 gas is used in the PECVD SiO_2 process.

[5] The thermal expansion coefficient of silicon is $2.6 \times 10^{-6}\ K^{-1}$ while that for SiO_2 is $0.5 \times 10^{-6}\ K^{-1}$ [31].

solid surfaces would allow for the post fabrication of the Peltier devices on them.[6]

SiO_2 diaphragms were fabricated as follows. 1.8 μm PECVD SiO_2 thin films were deposited on 3 inch <100> silicon wafers. These films were annealed for 20 minutes in a nitrogen ambient at 1100 °C to reduce stress. Backside etching of the silicon wafers was done in a 30 % KOH solution at 80 °C. This solution etches <100> silicon at a rate of 0.95 ± 16 % μm/min [32]. With a typical wafer thickness of 400 μm, the KOH etch takes approximately 6.5 hours to complete. To pattern the wafers for the backside etch, an appropriate masking layer for the back of the wafer is needed. A 0.5 μm thick PECVD Si_3N_4 thin film was chosen as the masking layer as it is very resistant to KOH etching.[7] The Si_3N_4 was photolithographically patterned, and a reactive ion plasma etch (RIE) was used to etch it to form the mask.

Of consideration in the KOH etch is the etch rate of the annealed PECVD SiO_2 used for the diaphragm. It was found that annealed PECVD SiO_2 etches at a rate of 0.0036 μm/min in KOH (a 260:1 ratio in the etch rates between silicon and annealed SiO_2). Therefore, during the seven hour etch approximately 1.5 μm of SiO_2 would be etched, a significant amount relative to the 1.8 μm SiO_2 thin film. To prevent damage to the SiO_2, a 0.5 μm thick PECVD Si_3N_4 thin film was deposited on the SiO_2 as a protective mask. This film was removed by RIE after completion of the backside etch.

Fabricated diaphragms possessed a high survivability but a rippled surface due to compressive stress present in the SiO_2. This rippled surface would make subsequent device processing on the diaphragm problematic. Further reduction in the stress of the SiO_2 diaphragm through annealing or PECVD chemistry manipulation was deemed too much effort. Consequently, the use of the SiO_2 diaphragms as the thermal isolation platform for the micro-Peltier pump was abandoned.

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[6] The solid diaphragm surface allows the spinning photoresist on it, thereby allowing photolithographic patterning of films subsequently deposited on it.

[7] A 0.2 μm PECVD Si_3N_4 thin film is sufficient for this length of KOH etch. However, due to the roughness of the backside of the silicon wafer a 0.5 μm thick film was used.

3.3.5 Cantilevers And Bridges

With the failure of microfabricated diaphragms, attention turned to cantilevers and bridges as the thermal isolation platform. Again, because a method to passivate the Bi_2Te_3 was not available at the outset of this thesis, post fabrication of the Peltier device is needed. How this is accomplished with cantilevers and bridges is the subject of section 3.3.6. This section will discuss stress differences between diaphragms, cantilevers, and bridges.

Microfabricated diaphragms suffer from two stress components. These are the intrinsic stress of the thin film making up their structure and thermal stress from the silicon wafer surrounding the diaphragm on its sides. Free standing cantilevers (and to a lesser degree bridges) differ from diaphragms in that they only suffer from the intrinsic stress of the thin film making up their structure. Fabricating cantilevers and bridges using PECVD SiO_2 films further reduces stress, as these films possess very little intrinsic stress [29]. Consequently, cantilevers and bridges fabricated from PECVD SiO_2 should not possess the rippled surface present in diaphragms, and should only possess a slight bend due to the small intrinsic stress present in the SiO_2.[8] A study was undertaken to determine the validity of this hypothesis.

Figures 3.6 and 3.7 are pictures of a cantilever and a bridge fabricated by photolithographic patterning and etching of rippled SiO_2 diaphragms. These figures show that the fabricated cantilevers and bridges do not possess the rippling present on the SiO_2 diaphragms from which they were fabricated. Significant misalignment is observed in these structures because the photolithography mask was aligned to the diaphragms by hand, because the mask aligner was not functioning on that particular day.

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[8] Bridges, having their two ends contacting the silicon wafer, can possess a bending component if sufficient compressive stress is forced upon them by the silicon wafer.

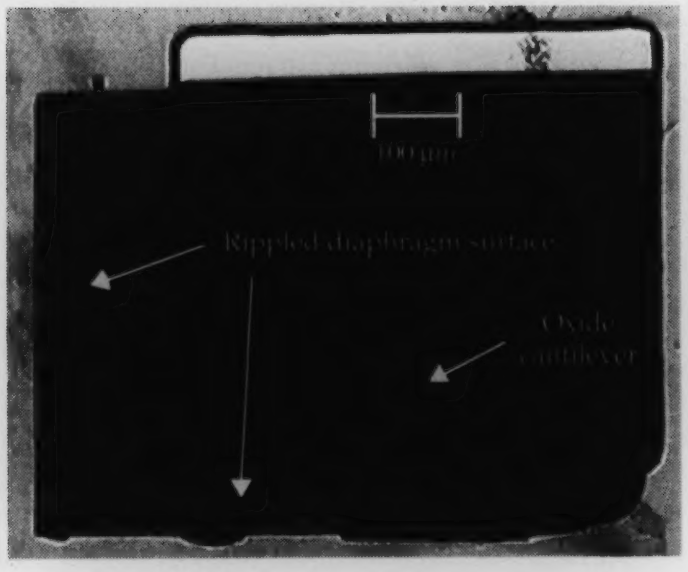


Figure 3.6: A 195 x 150 μm cantilever fabricated on a SiO_2 diaphragm surface.

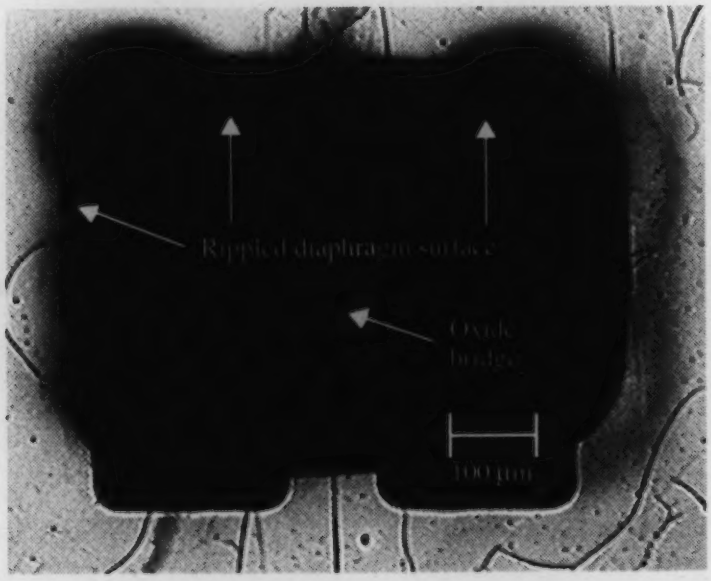


Figure 3.7: A 405 x 90 μm bridge fabricated on a SiO_2 diaphragm surface.

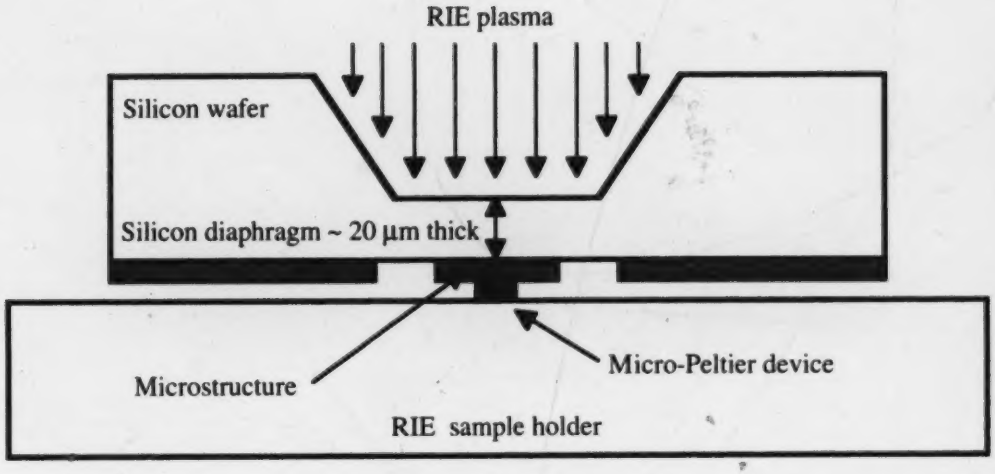
3.3.6 Backside Etched Cantilevers And Bridges

With the failure of the diaphragms as post fabrication platforms (see section 3.3.4), attention turned to microfabricated cantilevers and bridges. Post fabrication of devices on cantilevers and bridges is not possible, however, due to the etched gorge surrounding these microstructures (Photoresist will not spin evenly making photolithography impossible.). The solution to this problem is to fabricate the cantilevers and bridges using a backside etch, but to not fully free these structures.

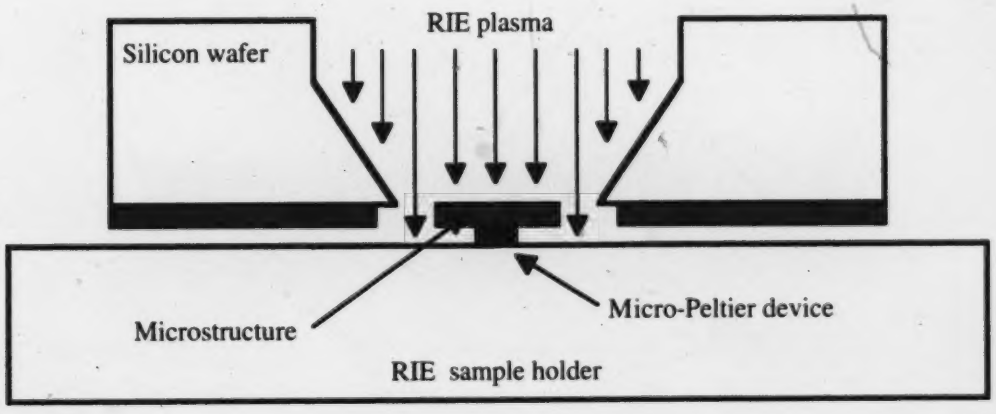
The fabrication of SiO_2 cantilevers and bridges by backside etching is done as follows. First, the SiO_2 thin film making up the microstructure is deposited. This is followed by a high temperature anneal in a nitrogen ambient to reduce stress. Next, a 0.5 μm Si_3N_4 thin film is deposited on both sides of the wafer. The backside Si_3N_4 is patterned beneath where the cantilever or bridge microstructure is to be located. The wafer is then etched until an ~ 20 μm thick silicon diaphragm remains. Next, the Si_3N_4 protecting the SiO_2 on the frontside of the wafer is removed by RIE. The SiO_2 is then patterned and etched into the desired microstructure shape. This step requires two sided photolithographic alignment between the cantilever or bridge mask on the front of the wafer and the etched silicon diaphragm on the back of the wafer.

After the above steps, the structure which remains is a patterned SiO_2 microstructure resting on an ~ 20 μm thick silicon diaphragm. This diaphragm is strong enough to possess a flat surface (no stress bending visible by microscope inspection) and to allow post fabrication of the Peltier device. After fabrication of the micro-Peltier pump, the final etch step is done, a release of the SiO_2 microstructure by a backside RIE of the silicon diaphragm (see Figure 3.8).

Figure 3.8 (a) shows the silicon wafer placed inverted on the sample holder of the RIE system. The RIE plasma attacks the wafer from the backside only precluding damage to the micro-Peltier pump on the frontside of the wafer. Figure 3.8 (b) shows the silicon wafer after the RIE plasma has etched through the silicon diaphragm. Since the reactive ion etch is anisotropic in nature (it etches primarily in the vertical direction), the plasma etch should not attack the micro-Peltier device because it is shielded by the microstructure. Therefore, passivation of the micro-Peltier pump should not be required.



(a)



(b)

Figure 3.8: Schematic of the backside etch process (not to scale). (a) shows the silicon wafer placed inverted on the sample holder of the RIE system. (b) shows the silicon wafer after the RIE plasma has etched through the silicon diaphragm.

3.4 Selection Of Materials For The Micro-Peltier Device

The micro-Peltier device is a two-junction Peltier heat pump (see section 2.4). As such, two materials are needed to form its thermoelectric junction. Since it is intended to be operated around room temperature, consideration was given to materials with a high figure of merit (z) at room temperature. This removed the alloys 88% Bi + 12% Sb, SiGe, and PbTe from the selection process (see Table 2.2). In addition to a high z, the ease of material deposition was considered. Therefore, complex alloys such as 90% Bi_2Te_3 + 5% Sb_2Te_3 + 5% Sb_2Se_3 were not considered.

The semiconductors Bi_2Te_3 and Sb_2Te_3 were investigated since they possess the highest z at room temperatures. Consideration was also given to antimony (Sb) and bismuth (Bi) due to their ease of deposition. Previously, they have been used to fabricate Sb-Bi thin film radiation sensors [8,33]. Table 3.1 lists calculated values for $z_{AB\,max}$ and maximum temperature differential (ΔT_{max}) for Peltier devices fabricated using various combinations of n-type Bi_2Te_3, p-type Sb_2Te_3, Sb, and Bi. P-type Bi_2Te_3 was not considered due to deposition difficulties[9]. Calculations were performed using Equations 2.30 and 2.33, and data from Table 2.2. Table 3.1 shows good performance is possible from Bi_2Te_3 - Sb_2Te_3, Bi_2Te_3 - Sb, and Sb_2Te_3 - Bi based devices.

Antimony is highly poisonous. Worse still, it will progressively accumulate in the body (in a similar manner to arsenic) until toxic levels are reached. Thus, continuous exposure (even in small doses) is inadvisable. Since the facilities at the Alberta Microelectronic Centre (AMC) are not suitable for working with this type of poisonous material, the fabrication of antimony based devices was rejected. Bismuth, tellurium, and Bi_2Te_3 are also toxic, but to a lesser degree.

The rejection of antimony left only Bi and n-type Bi_2Te_3 based devices possible. Due to the poor performance of Bi_2Te_3 - Bi devices, combinations of Bi_2Te_3 and Bi with the metals listed in Table 2.2 were considered. Calculated values for $z_{AB\,max}$ and ΔT_{max} are shown in Table 3.2. Good performance is apparent with Bi_2Te_3 in combination with any of the listed metals. Bismuth based devices were rejected because their potential

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[9] The deposition of n and p-type Bi_2Te_3 will be discussed in section 3.6.

performance is significantly poorer than Bi_2Te_3 based devices.

Table 3.1: Calculated values of $z_{AB\,max}$ and ΔT_{max} for Peltier devices fabricated using combinations of n-type Bi_2Te_3, p-type Sb_2Te_3, Sb, and Bi.

Material Combination	$z_{AB\,max}$ ($x10^{-3}$ K^{-1})	ΔT_{max} (K)
Bi_2Te_3 - Sb_2Te_3	1.88	84
Bi_2Te_3 - Bi	0.40	18
Bi_2Te_3 - Sb	1.3	59
Sb_2Te_3 - Bi	0.77	35
Sb_2Te_3 - Sb	0.19	8.6
Sb - Bi	0.29	13

Table 3.2: Calculated values of $z_{AB\,max}$ and ΔT_{max} for Peltier devices fabricated using n-type Bi_2Te_3 or Bi in combination with a variety of metals.

Material Combination	$z_{AB\,max}$ ($x10^{-3}$ K^{-1})	ΔT_{max} (K)
Bi_2Te_3 - Al	0.97	43
Bi_2Te_3 - Au	0.93	42
Bi_2Te_3 - Cr	0.88	39
Bi_2Te_3 - Mo	0.98	44
Bi_2Te_3 - W	0.81	37
Bi - Al	0.11	4.8
Bi - Au	0.11	5.1
Bi - Cr	0.14	6.3
Bi - Mo	0.13	5.7
Bi - W	0.095	4.3

3.5 Metals Used In The Fabrication Of The Micro-Peltier Pump

As indicated in Table 3.2, aluminum (Al), gold (Au), chrome (chromium, Cr), molybdenum (Mo), and tungsten (W) should all be acceptable materials for the fabrication of a room temperature Bi_2Te_3 based Peltier device. Sputtering was selected as the deposition technique for these materials.

Aluminum was the first metal used in prototype devices due to its wide usage in the semiconductor industry. Initial fabrication of Bi_2Te_3 - Al based Peltier devices was unsuccessful however. It was found that a Schottky contact is formed when Bi_2Te_3 is deposited on aluminum.[10] This type of contact is not acceptable for use with the micro-Peltier device. An ohmic contact is desired, as it results in a linear two-way heat pumping relationship.

With the failure of the aluminum based devices, gold was selected as the second thermoelectric material. Tests showed Bi_2Te_3 - Au contacts to be ohmic in nature. Other metals in Table 3.2 (Cr, Mo, and W) were not considered due to concerns of contact resistance between Bi_2Te_3 and these metals. Significant contact resistance will result in Joule heating which will adversely affect the performance of the Peltier pump. Gold, which lacks a surface oxide layer, should provide a superior electrical contact.

3.5.1 Adhesion Layers

The problem with gold metal is that gold does not adhere well to SiO_2. Consequently, the gold metallization would not adhere to the SiO_2 thermal isolation microstructure of the micro-Peltier device. Adhesion was promoted by depositing a thin adhesion layer between the gold metallization and the SiO_2. As will be mentioned in section 3.7, a second adhesion layer was deposited above the gold metallization. This allowed for the adherence of a SiO_2 passivation layer separating the gold metallization from the subsequently

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[10] The existence of this type of contact to Bi_2Te_3 has been seen before. Bi_2Te_3 deposited by thermal evaporation was found to react with silver and copper [34].

deposited Bi_2Te_3 film.

Three types of adhesion films (all deposited by sputtering) were experimented with for the various iterations of the micro-Peltier device. These were chrome, nichrome (NiCr), and molybdenum-tungsten, forming the structures Cr-Au-Cr, NiCr-Au-NiCr, and Mo-W-Au-W-Mo. These experiments are discussed further in section 3.8.6.

3.6 Bismuth Telluride Processing Details

This section will discuss details relating to the deposition and properties of Bi_2Te_3 thin films. A brief introduction to the semiconductor Bi_2Te_3 is presented below in order to familiarize readers with this material.

3.6.1 The Semiconductor Bismuth Telluride

Bismuth telluride (Bi_2Te_3) is a semiconductor with favorable thermoelectric properties. Because of this, bismuth telluride and its alloys have been the subject of a large number of investigations. Studies of bulk samples of Bi_2Te_3 have been carried out by [35-40]. Goldsmid [36] stated its energy gap (E_g) to be 0.16 eV, the mobility of electrons (μ_n) to be 430 cm^2 / Vsec, and that of holes (μ_p) to be 420 cm^2 / Vsec. Zone-refined (Czochralski method) polycrystalline and single crystal Bi_2Te_3 were found to possess identical properties. Crystalline Bi_2Te_3 possesses a rhombohedral crystal structure [40-41].

Bi_2Te_3 can be doped n or p-type by increasing or decreasing the tellurium concentration respectively about the stoichiometric ratio [41]. Satterthwaite et. al. [35] measured the room temperature thermoelectric power of Bi_2Te_3 as a function of the percentage of tellurium in the zone-refined melt (see Figure 3.9). Intrinsic Bi_2Te_3 was obtained at ~ 62.7 % tellurium, while stoichiometric composition is 60 % tellurium. In [41], it was stated that the reasons for intrinsic Bi_2Te_3 occurring at slightly above stoichiometric ratio are not fully understood. It may possibly be due to defects caused by the interchange of bismuth and tellurium atoms in the lattice.

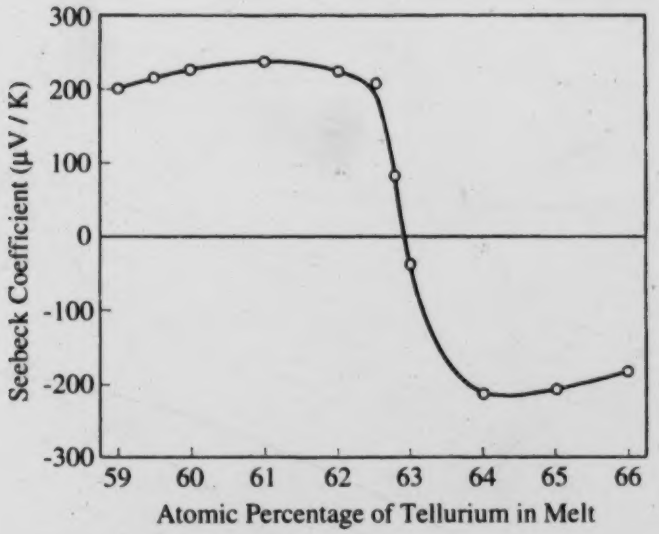

Figure 3.9: Room temperature thermoelectric power of Bi_2Te_3 as a function of the percentage of tellurium in the zone-refined melt [35].

Thin film depositions of Bi_2Te_3 have been performed by r.f. sputtering [42-43], and evaporation [34]. However, these processes often result in dissociation of the Bi_2Te_3 and a consequent lack of stoichiometry. Flash evaporation was used in [44]. In [6,9,45-48] co-evaporation was used to deposit stoichiometric Bi_2Te_3 thin films. Co-evaporation allows for the deposition of n or p-type Bi_2Te_3 through the control of the incident Te/Bi flux ratio onto the substrate.

Stoichiometric Bi_2Te_3 films were deposited by co-evaporation at flux ratios of Te/Bi ≥ 2 with substrate temperatures ≥ 250 °C.[11] At such elevated temperatures, tellurium does not stick to the substrate in an elemental phase, rather it deposits only in the

[11] It should be noted that in practice substrate temperatures are difficult to measure exactly. As such, there are some discrepancies in the literature.

compound Bi_2Te_3.[12] Charles et al. [46] observed that stoichiometric polycrystalline Bi_2Te_3 is formed when the substrate temperature is between 250 - 310 °C, and the ratio of incident fluxes is Te/Bi ≥ 2. 600 nm thick Bi_2Te_3 films deposited at substrate temperatures below 250 °C were found to have excess tellurium concentration, while those deposited at temperatures above 310 °C were found to be deficient in tellurium (see Figure 3.10).

Figures 3.11 (a) and (b) show measurements of carrier concentration, mobility, and Seebeck coefficients for the films. For stoichiometric films, the mobility was approximately five times lower than for single crystal films found by Goldsmid in [36]. Annealing samples at 420 °C for 1 hour had no effect on the Seebeck coefficient of films. Figures 3.11 (a) and (b) show favorable films to be deposited at a substrate temperature of 270 °C. George et al. [47] observed poor film adhesion at substrate temperatures below 530 K (257 °C), and discontinuous films at substrate temperatures above 545 K (272°C). The results of [46-47] suggest that an ideal substrate temperature would be in the range of 260 - 270 °C. Mzerd et. al [48] deposited Bi_2Te_3 films at temperatures 240 - 300 °C and found favorable films to be deposited at a substrate temperature of 270 °C. Films deposited by [46-48] possessed n-type doping due to excess tellurium in the films, with measured carrier concentrations on the order of 10^{20} cm^{-3}.

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[12] The temperature at vapour pressure (TVP) for bismuth and tellurium at 10^{-6} Torr (the approximate pressure of deposition) are 410 °C and 207 °C respectively [49]. Since the substrate temperature is higher than the TVP for tellurium (250 °C vs. 207 °C), elemental tellurium will re-evaporate off the substrate. However, the rate of this re-evaporation would have to be higher than the accumulation rate of free tellurium to preclude elemental tellurium agglomeration. The Hertz-Knudsen equation could be used to calculate the rate of tellurium re-evaporation [18].

$$\frac{dN}{Adt} = \alpha(2\pi mkT)^{-1/2}(p^* - p) \quad cm^{-2}sec^{-1} \qquad (3.1)$$

where N is the number of molecules, A is the thin film surface area, α is the evaporation coefficient (α ≤ 1) defined as the ratio of the observed evaporation rate to the value theoretically possible (This coefficient was Knudsen's contribution to Hertz's equation.), m is the mass of the molecule, k is Boltzmann's constant, T is the temperature in Kelvin, p^* is the equilibrium vapour pressure of the solid heated to temperature T, and p is the hydrostatic pressure acting on the surface (the return flux of the evaporant in the gas phase).

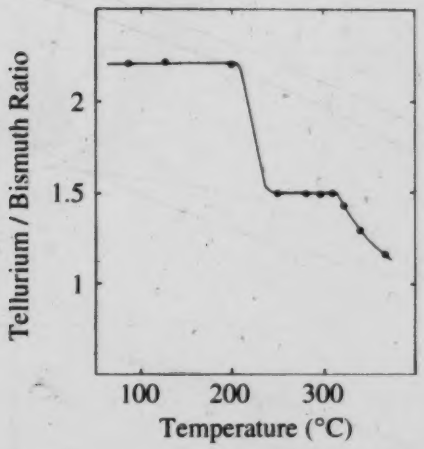

Figure 3.10: Atomic ratio of tellurium to bismuth in deposited films as a function of deposition temperature [46].

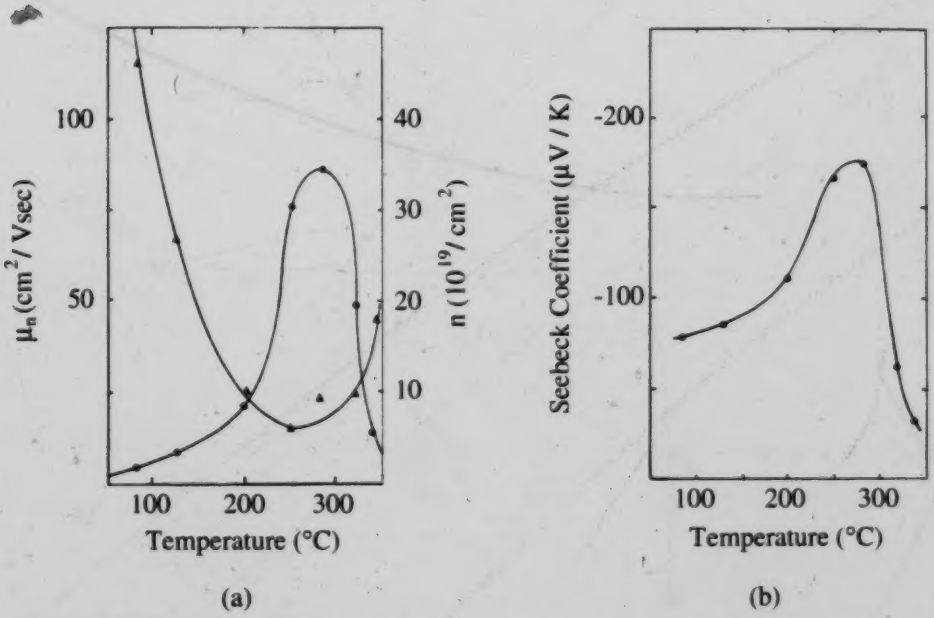

Figure 3.11: Deposited Bi_2Te_3 thin film properties with temperature [46]. (a) shows the variation in n-type carrier concentration (•) and electron mobility (▲). (b) shows the variation in the Seebeck coefficient.

3.6.2 Deposition Of Bismuth Telluride

Bismuth telluride thin films used for the micro-Peltier heat pump are deposited by co-evaporation. A vacuum system at the AMC (named Wilma) was modified to allow for the simultaneous usage of two evaporation sources. This involved the installation of two evaporation power supplies, two crystal thickness monitors, and the purchase of a stainless steel bell jar. The previous glass bell jar was unsuitable for this work. It possessed a small crack and it was felt that the high substrate temperature required for bismuth telluride deposition (260 - 270 °C) could possibly cause it to fail. A schematic of the deposition system is shown in Figure 3.12.

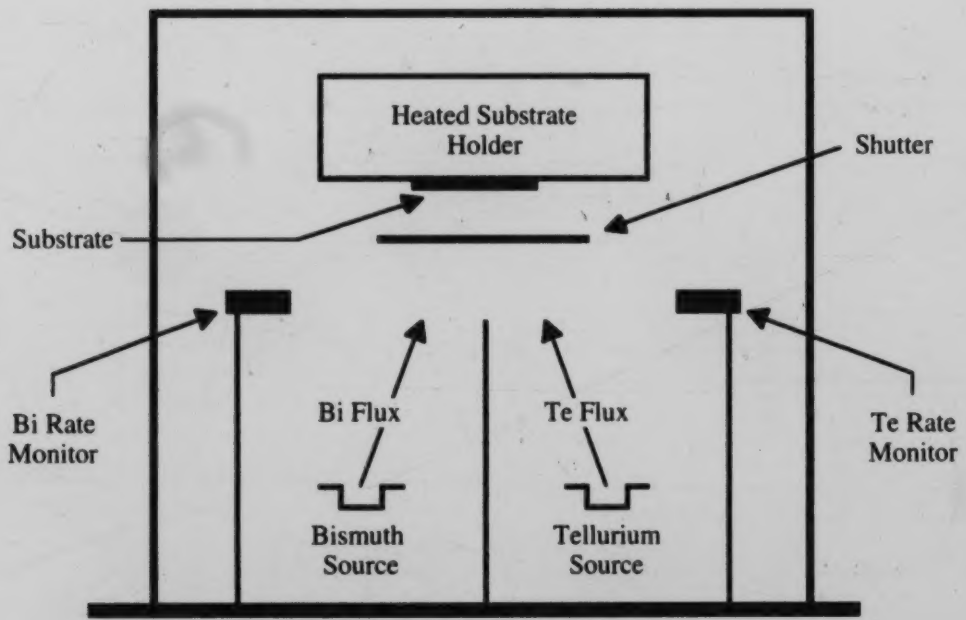

Figure 3.12: Schematic of the deposition system used for the co-evaporation of Bi_2Te_3.

3.6.3 Variation Of Bi_xTe_y Properties With Incident Te/Bi Flux

A study of how the resistivity and Seebeck coefficients of Bi_xTe_y films varied with the incident Te/Bi flux ratio was done in an effort to find a suitable ratio for the micro-Peltier heat pump. Suitable films must possess high Seebeck coefficient and low electrical resistivity. Bi_xTe_y films were deposited using high purity (99.999) bismuth and tellurium metals. The bismuth was evaporated from a molybdenum boat, and the tellurium was evaporated from a tungsten boat. Depositions were performed at a pressure of 2×10^{-6} Torr. Bi_xTe_y films were deposited on 0.6 μm thick silicon dioxide surfaces, which were grown thermally at 1100 °C on <100> silicon wafers (phosphorus doped, resistivity 1 - 10 Ωcm). The oxide films were used to electrically isolate the bismuth telluride films from the underlying silicon.

Bismuth telluride films were deposited at seven different Te/Bi flux ratios; 4:1, 3:1, 2.6:1, 2.5:1, 2.3:1, 2:1, and 1:1. The incident deposition flux rates were 5 - 6 Å/sec for bismuth and 5 - 24 Å/sec for tellurium depending on the film. The film thicknesses ranged from 0.68 μm to 1.1 μm. It is worth noting that although these films are of varying thicknesses, a comparison of their resistivities and Seebeck coefficients is valid as these properties stabilize for films possessing thicknesses above 0.5 μm [6]. A 1.48 μm thick Bi film was also deposited at room temperature for comparison.

The resistivities of the films were measured using a four point probe device, and their Seebeck coefficients were measured by the integral method. This method consists of a series of thermoelectric voltage measurements with both ends of the thermocouple held at a series of known temperatures (Two water baths were used as the thermal reservoirs.). For these measurements, a thermocouple was formed using the Bi_xTe_y thin film and an aluminum wire (99.999 purity). A Seebeck coefficient of -1.7 μV/°C [7] used for the aluminum wire was subtracted from the measurements to obtain the Seebeck coefficient of the Bi_2Te_3 film. Seebeck measurements showed all films to possess n-type doping. Measured resistivity and Seebeck values are shown in Table 3.3. A plot of these values is given in Figure 3.13.

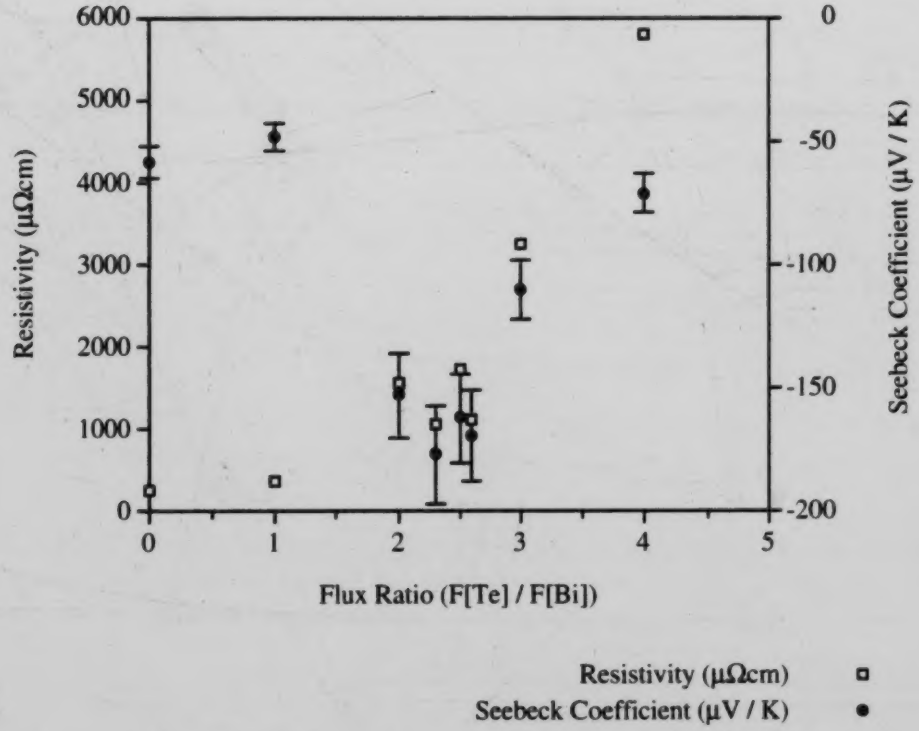

Figure 3.13: Measured resistivities and Seebeck coefficients for Bi_xTe_y thin films deposited at various values of incident deposition flux Te/Bi. The displayed error bars are due to measurement inaccuracy. Plotted data for the Te/Bi flux ratio of 2.3:1 are the average of the three 2.3:1 films of Table 2.3.

Films with a Te/Bi flux ratio of 1:1, 2:1, 2.3:1, 2.5:1, and 3:1 were deposited at substrate temperatures of 270 ± 1 °C. The F[Te] / F[Bi] = 2.6 film was deposited at a substrate temperature of 276 °C, and the F[Te] / F[Bi] = 4 film was deposited at a temperature of 265 °C.

Table 3.3: Measured resistivity and Seebeck coefficient for Bi_xTe_y thin films deposited at various values of incident deposition flux Te/Bi.

(F[Te] / F[Bi])	Run#	Thickness (μm)	Resistivity (μΩcm)	Seebeck Coefficient (μV / K)
0.0		1.48	269	-58
1.0		0.68	365	-48
2.0		0.67	1570	-153
2.3	1	1.1	1150	-187
	2	0.94	990	-184
	3	0.87	1030	-159
2.5		0.68	1717	-162
2.6		0.84	1105	-169
3.0		0.93	3250	-110
4.0		0.73	5800	-71

The Seebeck coefficient of the bismuth film in Table 3.3 agrees with that given in Table 2.2 and [17]. The measured electrical resistivity, however, differs from the value given for bulk bismuth in Table 2.2. This difference is reasonable as bulk resistivity is difficult to achieve in thin film materials due to surface and grain boundary scattering effects [50].

It can be seen from Figure 3.13 that the resistivities and Seebeck coefficients of the Bi_xTe_y films vary significantly with tellurium concentration. The Seebeck coefficient and resistivity are seen to increase from a pure bismuth film to that with F[Te] / F[Bi] = 1. This is due to the Bi_xTe_y film approaching stoichiometric from the p-doped side of Bi_2Te_3. The film F[Te] / F[Bi] = 2 possesses a large negative Seebeck coefficient as it is close to stoichiometric but on the n-doped side of Bi_2Te_3. It is expected that a p-type film can be deposited with the appropriate selection of deposition

fluxes somewhere in the range of 1 > F[Te] / F[Bi] > 2. The F[Te] / F[Bi] = 2.3 films possesses a more negative Seebeck coefficient and lower resistivity than the F[Te] / F[Bi] = 2 film due to an optimum concentration of n-type tellurium dopants. At F[Te] / F[Bi] > 3, large tellurium compositions lead to increasing Seebeck coefficients and resistivities, as pure tellurium possesses very poor conductivity.

Figure 3.13 shows that bismuth telluride films favorable for use in a Peltier device are deposited with F[Te] / F[Bi] = 2.3. The Seebeck coefficients and resistivity of this film agree with those of Table 2.2 and [6,9,45-46,48]. More precise optimization of the flux ratio was not possible with the equipment due to a lack of control of the deposition flux. It is for this reason that p-type Bi_2Te_3 films were not experimented with.

It is emphasized that the Te/Bi flux ratios presented in Table 3.3 and Figure 3.13 refer to the deposition flux incident on the substrate, not to the resultant film composition. The atomic ratio of bismuth and tellurium in the films was quantified using light atom Energy Dispersive X-ray Analysis (EDX) in a scanning electron microscope. The EDX analysis was performed at 15 kV for the films deposited at F[Te] / F[Bi] = 1, 2, 3, and 4. Results shown in Table 3.4 indicate that the atomic ratios of bismuth and tellurium in these films do not significantly differ from the incident flux ratio. The error in the bismuth and tellurium intensity measurements was less than 3 %.

Table 3.4: Measured atomic ratios of bismuth and tellurium in Bi_xTe_y thin films deposited at F[Te] / F[Bi] = 1, 2, 3, and 4.

(F[Te] / F[Bi])	Atomic Te/Bi Ratio
1	0.83:1
2	1.64:1
3	2.82:1
4	3.40:1

3.6.4 Importance Of Substrate Temperature

The substrate temperature during deposition must be noted in the interpretation of the results of Figure 3.13. This is because the rate of re-evaporation of elemental tellurium is dependent on temperature as given in Equation 3.1. Higher temperatures result in an increased rate of re-evaporation.

Films with a Te/Bi flux ratio of 1:1, 2:1, 2.3:1, 2.5:1, and 3:1 were deposited at substrate temperatures of 270 ± 1 °C. The F[Te] / F[Bi] = 2.6 film was deposited at a substrate temperature of 276 °C, and the F[Te] / F[Bi] = 4 film was deposited at a substrate temperature of 265 °C. These last two films experienced noticeably different tellurium re-evaporation rates. The F[Te] / F[Bi] = 2.6 film experienced a higher re-evaporation rate, and the F[Te] / F[Bi] = 4 film experienced a lower re-evaporation rate. The higher re-evaporation rate of the F[Te] / F[Bi] = 2.6 film resulted in a decreased tellurium concentration in the film, which explains the errant nature of its data point on Figure 3.13. From the pattern of the other data points, the resistivity and Seebeck coefficient of this film are what would be expected from a film deposited at an incident flux ratio close to 2.3:1.

3.6.5 Lateral Uniformity Of Bi_xTe_y Films

Of concern with co-evaporation is the compositional uniformity of the deposited film across the substrate width. Differences in the distance and angles of incidence from the two evaporation sources (see Figure 3.12) to locations on the substrate results in chemically non-homogenous films. As the properties of Bi_xTe_y are dependent on its level of doping, small variations in film composition can result in significant differences in its properties.

One can calculate the differential deposition rate of an evaporant stream on a substrate using (see Figure 3.14) [18],

$$\frac{dM_r(\phi,\theta)}{dA_r} = \frac{M_e}{\pi r^2}\cos(\phi)\cos(\theta) \qquad (3.2)$$

where M_e is the total mass evaporated from the source A_e. For example, using Equation 3.2 with the dimensions of the Wilma vacuum system used for this thesis, the variability across an ~ 1 inch wide substrate would be ~ 3 %. Equation 3.2, however, is somewhat simplistic in that it assumes that the distribution of the evaporant stream follows the function cos(ϕ), which relates to a point source of evaporant. This assumption may not be valid for a boat evaporation source, where the source material can evaporate more evenly in the sideways direction.

In order to minimize non-homogeneity of the Bi_xTe_y films for this thesis, care was taken to position the micro-Peltier device along the central axis between the two evaporation sources.

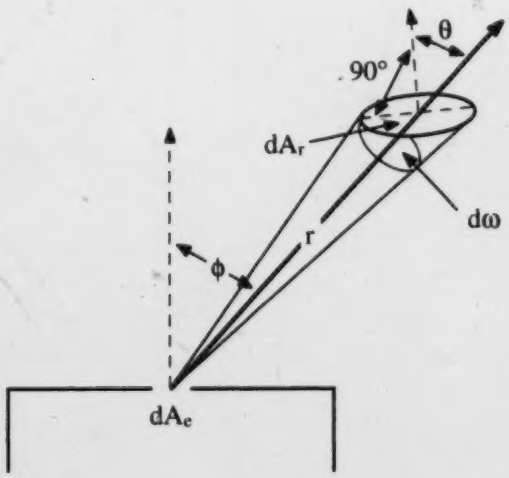

Figure 3.14: Differential deposition rate of an evaporant stream on a substrate as a function of incident angles θ and ϕ [18].

3.6.6 Depth Uniformity Of Bi_xTe_y Films

It should be mentioned that the incident fluxes of bismuth and tellurium forming the Bi_xTe_y films deposited in this thesis were controlled manually. Incident deposition rates were monitored by the crystal thickness monitors, and the currents to the evaporation boats were manually adjusted to maintain desired deposition fluxes. The unsteadiness of the flux control with this technique had the consequence of variable Bi_xTe_y film composition throughout the film thickness. Te/Bi flux ratios are calculated from the final film thicknesses measured by the crystal thickness monitors. Thus, the Te/Bi flux ratios presented in this thesis are the average flux throughout the duration of deposition, not the absolute flux.

3.6.7 Oxygen Impurity Level In The Bi_xTe_y Films

With the moderate deposition pressures of the above Bi_xTe_y films (2×10^{-6} Torr), the presence of impurities in the films is of concern. Of primary concern is oxygen as both bismuth and tellurium will react with it. At 2×10^{-6} Torr, the impingement rate of background species in the vacuum system is on the order of 1 monolayer per second,[13] while the incident flux rates are 5 - 6 Å/sec for bismuth and 5 - 24 Å/sec for tellurium.

In an attempt to quantify the level of oxygen impurity, the bismuth telluride film deposited at F[Te] / F[Bi] = 2.3 in Run# 2 was analyzed using EDX.[14] The EDX

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[13] The monolayer formation time can be found from (This equation assumes all incident molecules stick to the substrate.)[50],

$$\tau_m = \left(\frac{dN}{Adt}\right)^{-1} p_a = \frac{(2\pi mkT)^{1/2}}{p} p_a \quad \text{seconds} \qquad (3.3)$$

where $\frac{dN}{Adt}$ is the impingement rate on the surface [18], N is the number of molecules, A is the thin film surface area, m is the mass of the impinging molecules, k is Boltzmann's constant, T is the temperature in K, p is the vacuum chamber pressure, p_a is the atomic packing density on the substrate. For N_2 gas at 2×10^{-6} Torr, $p_a = 8 \times 10^{14}$ cm^{-2} [18]. Thus, $\tau_m \sim 1$ second.

[14] The incident flux ratio of F[Te] / F[Bi] = 2.3 is the ratio used to deposit the Bi_2Te_3 thin films for the micro-Peltier device.

compositional analysis was performed at 15 kV and the bismuth-tellurium-oxygen intensity results (normalized to 100) showed the oxygen intensity to be 1.2 ± 0.6 % (the error is 2 standard deviations), resulting in an atomic percentage of 11 % oxygen. It should be noted, however, that no oxygen peak was visible in the intensity spectrum (The oxygen reading was within the measurement noise level.). Also, measurement resolution of EDX for oxygen is nominally only a few percent. Thus, no quantitative conclusion can be made as to the oxygen level. Since the Seebeck coefficient and resistivity for the F[Te] / F[Bi] = 2.3 Bi_xTe_y films are consistent with those of Table 2.2 and [6,9,45,46,48], it is assumed that the presence of oxygen does not deleteriously affected the films.

3.6.8 Microstructure Of Thin Film Bi_2Te_3

Figure 3.15 is SEM picture of the cross-section of a Bi_2Te_3 film deposited at a Te:Bi flux ratio of 2.3:1. The large grained polycrystalline microstructure of this film is consistent with the high temperature of deposition.

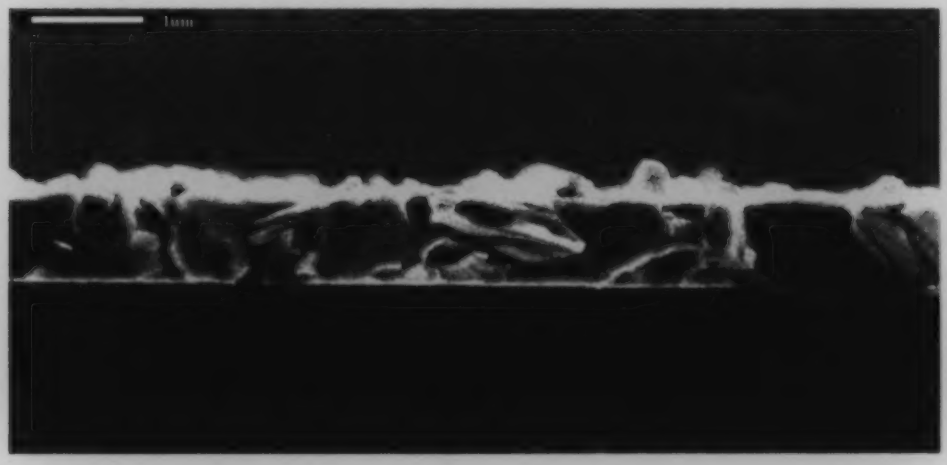

Figure 3.15: Microstructure of thin film Bi_2Te_3 deposited at a Te:Bi flux ratio of 2.3:1.

3.7 Processing Steps For Device Fabrication

The processing steps used in the fabrication of the micro-Peltier pump are shown in Figure 3.16 and are discussed below.

Step 1: A PECVD SiO_2 thin film is deposited at 350 °C onto the frontside of a 3 inch <100> silicon wafer. This film forms the thermally isolated microstructure upon which the Peltier Device is fabricated. The thickness of this film varied with each iteration of the micro-Peltier device, and ranged from 1.5 - 1.8 µm.

Step 2: The SiO_2 film is annealed at 1100 °C for 20 minutes in a nitrogen ambient to reduce stress (see section 3.3.1).

Step 3: 0.5 µm PECVD Si_3N_4 thin films are deposited on both sides of the silicon wafer (see Figure 3.16a). The backside film serves as an etch mask for the backside of the wafer when forming the silicon diaphragms (see section 3.3.4). The frontside film protects the SiO_2 during the backside etch.

Step 4: **Mask 1**. The backside Si_3N_4 is photolithographically patterned and etched (using RIE) to form the backside etch mask.

Step 5: The wafer is etched in a 30 % KOH solution at 80 °C until an ~ 20 µm thick silicon diaphragm remains (see Figure 3.16b). The diaphragm thickness is controlled by precise timing of the KOH etch, and is verified by inspection using a microscope with a focus dial possessing micron graduations. The etch time is ~ 6.5 hours.

Step 6: The Si_3N_4 protecting the SiO_2 on the frontside of the wafer is removed by RIE.

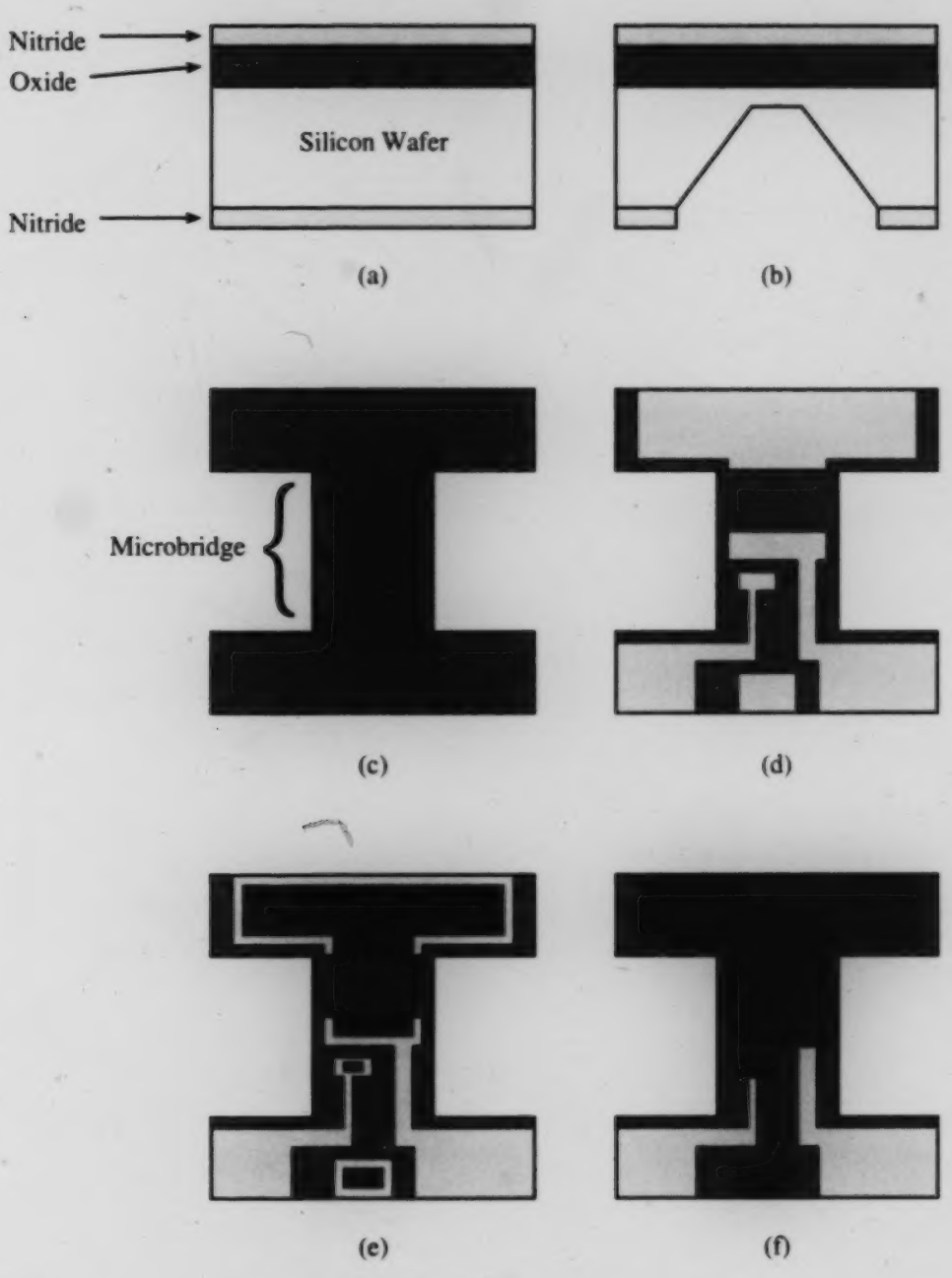

Figure 3.16: The main processing steps in the fabrication of the micro-Peltier pump.

Step 7: **Mask 2**. The SiO_2 is patterned and etched in 10 : 1 Buffered Oxide Etch (BOE) into the desired microstructure shape upon which the micro-Peltier pump will be fabricated. This step requires two sided photolithographic alignment between the microstructure mask on the front of the wafer and the etched silicon diaphragm on the back of the wafer. Figure 3.16c shows a top view of the patterned SiO_2 forming a microbridge.

Step 8: The gold metallization layer is deposited by sputtering. The thickness of this film varied with each iteration of the micro-Peltier device, and ranged from 0.1 - 0.25 μm. It should be noted that the underlying SiO_2 acts as a barrier to gold diffusion into the silicon.

As indicated in section 3.5, adhesion materials were deposited on either side of the gold metallization. Chrome, Nichrome, and Molybdenum-Tungsten were each used forming the structures Cr-Au-Cr, NiCr-Au-NiCr, and Mo-W-Au-W-Mo. Film thicknesses used were 500 Å of chrome, 300 Å of nichrome, and in the molybdenum-tungsten case, 200 Å of molybdenum and 300 Å of tungsten.

Step 9: **Mask 3**. The gold metallization is patterned and etched to form the electrical conduction lines for the Peltier device and a thermocouple (see Figure 3.16d). The thermocouple is used during testing to measure the temperature differential produced by the Peltier device.

Step 10: A PECVD SiO_2 film is deposited over the gold metallization. This film is used to passivate the gold metallization from the subsequent Bi_2Te_3 deposition. The thickness of this film varied with each iteration of the micro-Peltier device, and ranged from 0.3 - 1 μm.

Step 11: **Mask 4**. The PECVD SiO_2 film is patterned and etched in 10 : 1 BOE to form via contacts to the underlying gold metallization (see Figure 3.16e).

Step 12: The exposed adhesion metal on top of the gold metallization at the bottom of the via contacts is removed. This will allow for good contact between the gold metallization and the Bi_2Te_3 deposited in step 14.

Step 13: **Mask 5**. The PECVD SiO_2 film deposited in step 10 is again patterned and etched in BOE to form via contacts to wire bonding pads used for device testing. The exposed adhesion metal at the bottom of these via contacts is not removed (Thus, different lithography masks are needed for steps 11 and 13.). This is because the etchant for the Bi_2Te_3 (used in step 15) will also remove exposed gold metallization. The exposed adhesion metals at the via bottoms (Cr, NiCr, or Mo-W) etch much slower than Bi_2Te_3 and so protect the gold metallization beneath them.

For the first device prototypes, the SiO_2 thermal isolation microstructure was re-patterned in this process step as well. As will be explained in section 3.8.7, this was not done for later devices.

Step 14: The Bi_2Te_3 material is deposited at a flux ratio of Te/Bi = 2.3. Film thickness ranged from 0.9 - 1.1 μm for the various Peltier device prototypes.

Step 15: **Mask 6**. The Bi_2Te_3 film is lithographically patterned and etched in a solution of nitric acid (HNO_3), hydrogen chloride (HCl), and water (H_2O) with the ratio 2 HNO_3 : 1 HCl : 1.5 H_2O (see Figure 3.16f).

Step 15a: The final study of this thesis involved the deposition of a SiO_2 passivation film on the Bi_2Te_3. Both PECVD and sputtered SiO_2 films were investigated with thicknesses ranging from 1 - 1.5 μm.

Step 15b: The SiO_2 passivation film is patterned and etched in 10 : 1 BOE using mask 5 to expose via contacts to the wire bonding pads used for device testing.

Step 16: The silicon diaphragm is etched from the backside of the wafer using RIE (see Figure 3.8) to free the SiO_2 thermal isolation microstructure.

3.8 Other Processing Details

Specific processing issues studied during the fabrication of the micro-Peltier pump are discussed in this section.

3.8.1 Adhesion Of Bi_2Te_3

Bi_2Te_3 does not adhere well to SiO_2. It will not survive the "Scotch Tape Test" [18], and will separate from a SiO_2 substrate under the aggressive spraying of liquids from a squeeze bottle. Also, stress bending of the substrate may result in the separation of the Bi_2Te_3 film deposited on it. This is somewhat aggravated by the stiffness of the Bi_2Te_3 film. In spite of these problems, Bi_2Te_3 will survive the stress of photoresist spinning, developing, and post-etch resist removal with acetone. In the latter case, resist removal is done by an acetone soak (1 minute) not by spraying from a squeeze bottle, as this may remove the Bi_2Te_3. Blow drying the acetone is not recommended, since it results in a rapid temperature drop (due to acetone evaporation) which can result in Bi_2Te_3 separation from the substrate due to thermal stress. Acetone removal is accomplished by dipping the acetone coated substrate in water, followed by gentle blow drying of the acetone-water mixture off the substrate. The lesser temperature drop resulting with this technique will not result in Bi_2Te_3 separation from the substrate.

Bi_2Te_3 adheres very well to gold due to inter-diffusion between these materials during the elevated temperature of the Bi_2Te_3 deposition. Bi_2Te_3 - gold inter-diffusion is discussed further in section 3.8.4.

Bi_2Te_3 adheres poorly to silicon and chrome. The Bi_2Te_3 film will separate from

these materials under the stress of photoresist spinning when attempting to pattern it. Consequently, all silicon and chrome surfaces of significant size (greater than 500 x 500 μm) are coated with SiO_2.

Soaking PECVD SiO_2 substrates in HNO_3 for 2 minutes is found to prevent subsequent Bi_2Te_3 film adhesion. HNO_3 soaked substrates cleaned in cold piranha etch for 10 minutes have no subsequent adhesion problems. These observations were not investigated further.

Bi_2Te_3 does not adhere to PECVD SiO_2 after coated substrates have been stored in plastic sample dishes. Glass or teflon sample dishes do not appear to be a problem. It is suspected that organic contamination from the plastic finds its way to the SiO_2 surface in vapour form, resulting in an adhesion inhibitor. Soaking the samples in acetone, HNO_3, or room temperature piranha etch (a mixture of sulfuric acid and hydrogen peroxide with the ratio 3 H_2SO_4 : H_2O_2) for up to 20 minutes did not solve this problem. A 10 second dip of the substrate in 2 HNO_3 : 1 HCl solved this problem, but this method is not usable since this solution also etches exposed gold metal.

Organic contamination of silicon wafers from plastic containers was investigated in [51]. The authors found that fuming nitric acid or piranha etch was incapable of fully removing organic contaminants. Dilute hydrofluoric acid (HF) and ozonized water (O_3/H_2O) were successful, however.[15] These solutions were not investigated in this thesis.

3.8.2 Etching Of Bi_2Te_3

A solution of HNO_3, HCl, and water with the ratio 2 HNO_3 : 1 HCl : 1.5 H_2O is successful in etching photolithographically patterned Bi_2Te_3. The solution 2 HNO_3 : 1 HCl is made first. After about 15 minutes when the solution's color stabilizes

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[15] Dilute hydrofluoric acid (HF) removes organics through the removal of surface oxides. Ozonized water (O_3/H_2O), with its very high oxidation potential, was found to successfully remove organics [51].

to deep red, the H_2O dilution is added (Addition of the H_2O prior to this color stabilization will make a poorer quality etchant.).

This solution etches Bi_2Te_3 quickly and violently. A 1 μm thick film etches in about 8 seconds with minimal undercut seen on patterned 15 μm features. The etching is associated with the release of bubbles foaming off of the film (and possibly out of the beaker containing the solution). Consequently, only small substrate pieces (less than 4 cm^2) should be immersed in the etchant. Etch completion occurs when the violent bubbling action stops, at which time the substrate piece is immediately dipped in water to stop the etching and so minimize undercutting of the photoresist mask. Some residue is occasionally seen on the substrate after Bi_2Te_3 etching. This residue is removed when the acetone soak (1 minute) is used to remove the photoresist mask.

It should be noted that fumes coming off this etchant will also etch Bi_2Te_3. Thus, samples should not be held above the etchant for any length of time. The etching of Bi_2Te_3 also releases toxic gasses. All etching was performed under a fume hood.

Adding more HCl to the above etchant is found to unfavorably increase the etch rate of Bi_2Te_3. Pure 2 HNO_3 : 1 HCl etches Bi_2Te_3 too quickly (a 1 μm thick film etches in about 5 seconds) resulting in occasional crack failures appearing in patterned regions of the Bi_2Te_3, possibly due to stresses incurred during etching. Dilutions of 2 HNO_3 : 1 HCl with greater than 1.5 H_2O etch Bi_2Te_3 too slowly, allowing sufficient time for lift-off of the film from the substrate.

Bi_2Te_3 is not attacked by a solution of 10 : 1 BOE in a 1 minute exposure. This fact may be of interest for process compatibility with SiO_2 passivation films.

SF_6 plasma will etch Bi_2Te_3 in RIE. The etch rate was found to be 0.5 μm/min for a 25 % flow, at 60 mTorr, and a power of 62 W. No attempt was made to investigate this further or use this etch technique in device fabrication.

A Bi_2Te_3 film will be lifted-off from a substrate by nitric acid in about 20 seconds and by cold piranha etch in about 2 minutes. It will be attacked by chrome etch with a non-uniform etch rate of about 100 nm/minute.

3.8.3 Metal Etching Concerns

Gold was etched in KI_3 (potassium iodide/iodine) gold etchant. Aqua regia was not used due to the greater amount of undercut of the photoresist mask.

Cr and NiCr were etched using standard chrome etchant (Olin Microelectronic Materials Chrome Etch.).

Mo-W was etched in H_2O_2. The 200 Å Mo - 300 Å W film etched in ~ 30 seconds. Due to the adhesion layers on either side of the gold metallization, two H_2O_2 etches were needed, totalling one minute in time. The photoresist mask[16] started to be attacked by the H_2O_2 during this extended time period. The etch was, however, completed successfully with no measured loss of photoresist thickness.

BOE will attack Mo-W. A 5 minute etch in 10 : 1 BOE was found to remove approximately half the thickness of the 200 Å molybdenum film. The tungsten film was found untouched by the BOE during this time period. This result is significant as it shows the Mo-W film capable of surviving the BOE etch used to form the via contacts to the wire-bonding pads (step 13 in section 3.7).

The Bi_2Te_3 etchant will attack NiCr and Mo-W. After 10 seconds in the etchant, the 300 Å NiCr film was noticeably pin-holed, and after 20 seconds it was mostly removed. After 30 seconds in the etchant, the 200 Å molybdenum film was mostly gone, but the underlying tungsten film remained intact. These results are significant as they show the NiCr and Mo-W films capable of protecting the gold metal at the vias to the wire-bonding pads during the Bi_2Te_3 etch, which is only ~ 8 seconds in length.

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[16] Olin HPR 506 photoresist spun at 3000 rpm was used as the etch mask. Resist thickness was measured to be 2.5 µm after hard baking at 120 °C for 3 minutes.

3.8.4 Bi_2Te_3 - Gold Inter-Diffusion

The elevated temperature of the Bi_2Te_3 deposition results in the Bi_2Te_3 inter-diffusing with the gold metal. It is the inter-diffused nature of the Bi_2Te_3 - Au contact which is responsible for its ohmic nature. In order to determine the thickness of this inter-diffused region, the Bi_2Te_3 film was etched away (performed separately with nitric acid and piranha etch). The thickness of the remaining inter-diffused alloy was measured using a profilometer (alpha-step® 200, Tencor Instruments) and was found to be ~ 200 nm.

The inter-diffused alloy cannot be etched by nitric acid or piranha etch, both of which will etch Bi_2Te_3 but not gold. The alloy can be removed by 2 HNO_3 : 1 HCl which etches both Bi_2Te_3 and gold.

3.8.5 Resistivity Of The Gold Metallization

The optimal design of the micro-Peltier device (discussed in Chapter 4), with respect to Joule heating and thermal conduction losses, requires precise dimensional selection for the gold metal wiring. This requires knowledge of the resistivity of the gold thin film, as this will differ from the resistivity of bulk gold.

Table 3.5 shows the resistivity of gold thin films measured at a variety of thicknesses using a 4 point probe. The resistivity of bulk gold (see Table 2.2) is shown for comparison. Gold films were deposited by sputtering on annealed PECVD SiO_2 films on a silicon wafer. 300 Å thick chrome thin films were used to adhere the gold to the SiO_2. Because of the relatively high resistivity of the chrome thin films[17], their presence will not introduce significant error to the measured gold resistivities. It can been seen in Table 3.5 that the resistivity of thin film gold is higher than that of bulk gold. Bulk resistivity is difficult to achieve in thin film materials due to surface and grain boundary scattering effects [50].

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[17] The resistivity of a 0.5 µm sputtered chrome film was measured to be 56 µΩcm. The 300 Å chrome adhesion film should possess a higher resistivity.

Table 3.5: Measured resistivity of gold thin films.

Thickness (μm)	Resistivity (μΩcm)
0.11	6.2
0.15	5.0
0.25	4.5
0.4	4.9
Bulk Gold	2.35

3.8.6 Adhesion Metals And Gold Inter-Diffusion

Chrome, nichrome, and Mo-W were all experimented with as adhesion materials for the gold metallization.

Chrome was used initially. It was found, however, that chrome inter-diffuses with gold during the elevated temperatures of the PECVD SiO_2 process (350 °C) and the Bi_2Te_3 deposition (270 °C). The result being that the gold metallization increases in resistivity by a factor of about 7, with a resulting loss of device performance due to excessive Joule heating. This inter-diffusion is visible as a color change of the gold metallization toward a more silvery color.

Nichrome was substituted in an attempt to reduce the gold inter-diffusion. Significant inter-diffusion did occur, however, with an increased resistivity of the gold metallization by a factor of about 2.

Molybdenum-tungsten was subsequently evaluated as an adhesion material. No increase in gold resistivity was observed after annealing at temperatures up to 350 °C [52] (350 °C is temperature of the PECVD SiO_2 process.). Mo-W is the adhesion material that should be used in all future iterations of the micro-Peltier device.

3.8.7 Damage To The Bi_2Te_3 During RIE Backside Etch

The RIE of the silicon diaphragm (step 16 in section 3.7) was seen to result in damage to the Bi_2Te_3 film in the first device prototypes. This damage took the form of crack failures and occasional separation of the Bi_2Te_3 film from the substrate. Two effects were thought to be the cause of the damage. They are the etching of the Bi_2Te_3 film by the SF_6 plasma, and bending of the SiO_2 microbridge after its release.

Etching The Bi_2Te_3 Film:

In section 3.3.6, it was stated that the RIE plasma should not attack the micro-Peltier device after the silicon diaphragm is etched away. This assumption was found to be wrong. A method to protect the Peltier device after the removal of the silicon diaphragm was then devised.

It was decided that the 0.3 µm thick passivation oxide would not be re-patterned to form the SiO_2 microbridge (step 13 section 3.7). This results in a thin SiO_2 diaphragm surrounding the microbridge. This diaphragm protects the Peltier device after the silicon diaphragm is etched away. After the silicon etch, the SiO_2 diaphragm can be etched away in a short duration RIE or BOE etch if so desired.

It should be noted that the presence of the SiO_2 diaphragm will reduce the thermal isolation of the Peltier device. This is discussed in section 4.4.

Bending Of The Microbridge:

A slight bend is visible in the SiO_2 microbridge after it is freed from the underlying silicon diaphragm. This bending could be due to stress inherent in the SiO_2 film or differential stress between the SiO_2 and Bi_2Te_3 films. This bending may be a primary cause of the observed damage to the Bi_2Te_3 film. This stress bending could possibly be solved by experimenting with the SiO_2 deposition process in order to deposit films with different stress levels. This was not investigated in this thesis.

Heating Of The SiO_2 Microbridge:

A third effect which was thought responsible for damage to the Bi_2Te_3 film is the stress due to heating of the SiO_2 microbridge by the RIE plasma. The temperature of the microbridge will rise once the underlying silicon diaphragm is etched away, since the high thermal conductivity of the silicon no longer helps heat sink the device.

The temperature increase of the microbridge is estimated to be only ~ 25 °C above that of the bulk silicon wafer.[18] It is felt that this temperature increase is not sufficient to cause thermal stress damage to the Bi_2Te_3 film. Therefore, thermal stress due to the RIE etch is felt to not be a problem.

3.9 Passivating The Bi_2Te_3 Thin Film

The final processing study of this thesis was the investigation of SiO_2 passivation for the micro-Peltier pump. A passivation film would protect the Bi_2Te_3 film and the Peltier device, and allow for future processing steps after device fabrication. Both PECVD and sputtered SiO_2 films were investigated.

Bi_2Te_3 - Au devices (Bi_2Te_3 wires with gold contact pads at each end) were fabricated for this study. A 1.5 µm thick PECVD SiO_2 thin film was deposited on a silicon wafer. A sputtered NiCr - Au - NiCr film (thickness 300 Å - 0.25 µm - 300 Å) was then deposited and patterned. This film was passivated by a 0.3 µm thick PECVD SiO_2 film. After the etching of appropriate via holes, a 1 µm thick Bi_2Te_3 film was deposited at a flux ratio of F[Te] / F[Bi] = 2.3. This film was patterned to form Bi_2Te_3 wires. A 1 µm thick PECVD or sputtered SiO_2 was then deposited over the devices. The criterion for successful passivation was deemed to be no (or minimal) change in the

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[18] The temperature increase of 25 °C is determined as follows. First, the power incident on the SiO_2 microbridge is determined by dividing the total power of the RIE plasma (60 W) by the ratio of the surface areas of the SiO_2 microbridge (570 x 270 µm) and the RIE chuck (6 inch diameter). The resulting power is then divided by the thermal conductivity of the SiO_2 microbridge (~ 20 µW/°C as given in section 4.4).

resistivity of the Bi_2Te_3 - Au devices as measured before and after SiO_2 passivation.

3.9.1 PECVD SiO_2 Passivation

A 1 μm thick PECVD SiO_2 film was deposited at 350 °C. The resistance of the Bi_2Te_3 - Au devices decreased significantly after passivation (see Table 3.6). The decrease in resistance is due to diffusion of gold metal into the Bi_2Te_3 at the elevated temperature of the PECVD deposition step. This diffusion, beyond the normal gold diffusion during Bi_2Te_3 deposition, is understandable as the PECVD deposition temperature (350 °C) is greater than the Bi_2Te_3 deposition temperature (270 °C). This technique of passivation was abandoned due to the marked change in device resistance.

Table 3.6: Measured resistance of the Bi_2Te_3 - Au devices before and after PECVD SiO_2 passivation. Measurement error is less than 0.5 Ω.

Bi_2Te_3 Wire		Resistance (Ω)	
		Before Passivation	After Passivation
120 x 180 μm	#1	22.0	13.8
	#2	21.3	11.7
	#3	22.3	12.1
	#4	21.5	11.7
120 x 120 μm	#1	32.3	18.2
	#2	30.8	17.1
	#3	32.4	18.5
	#4	30.8	17.6

3.9.2 SiO_2 Passivation Deposited By Sputtering

SiO_2 can be deposited by sputtering. The substrate will increase in temperature during the sputtering process due to bombardment by ions, electrons, and energetic neutrals. However, the process used for the sputtered SiO_2 will not increase the substrate temperature significantly (less than 100 °C [52]). Therefore, the thermal diffusion failures seen in the PECVD SiO_2 process should not occur. A reactive pulsed DC sputtering process was selected due to its faster rate of SiO_2 deposition in comparison to standard RF sputtering. In this process, sputtered silicon is reacted with oxygen gas to form the SiO_2. This process and processing experiments with the deposited SiO_2 films are discussed in detail in Appendix C.

The etch properties of the SiO_2 film deposited on wafer 4 of Run* 2 (see Appendix C) resulted in its selection for the passivation film. Table 3.7 shows the resistance of the Bi_2Te_3 - Au devices before and after passivation by a 1 μm thick SiO_2 film. Although the resistance of the devices changed, the change is minimal and so this process is felt acceptable for use as passivation.

Table 3.7 also shows results for the subsequent deposition of a 1 μm PECVD SiO_2 film (deposited at 350 °C) on the passivated Bi_2Te_3 - Au devices. It can be seen that the elevated temperature of this process again significantly affects the Bi_2Te_3 - Au devices.

Table 3.7: Measured resistance of the Bi_2Te_3 - Au devices before and after sputtered SiO_2 passivation, and coating by a 1 μm PECVD SiO_2 film. Measurement error is less than 0.5 Ω.

Bi_2Te_3 Wire		Resistance (Ω)		
		Before	After Sputtered SiO_2	After PECVD SiO_2
240 x 180 μm	#1	144	154	failed device
	#2	114	163	failed device
	#3	44.1	48.8	23.6
	#4	35.3	35.8	failed device
120 x 180 μm	#1	19.8	19.3	9.9
	#2	21.6	22.5	15.7
	#3	19.8	18.9	9.1
	#4	19.0	16.9	9.5
120 x 120 μm	#1	28.8	26.3	13.1
	#2	24.5	23.5	13.4
	#3	28.2	27.3	13.0
	#4	24.8	23.5	12.8

Chapter 4

SIMULATED AND MEASURED PERFORMANCE

> "It is only at long intervals that the researcher enjoys the feeling (or illusion) of solid accomplishment that the administrator can enjoy merely by emptying his in-box."
>
> -- Spencer Klaw

4.1 Introduction

This chapter describes the device model used to estimate the performance of the micro-Peltier pump. This model is constructed using the theories and material properties presented in Chapters 2 and 3. Calculations from this model are compared to measured performance results for a device prototype. Measured results for other prototypes are given.

4.2 Properties Used In Performance Estimates

The maximum temperature differential possible with various material choices for the micro-Peltier pump is calculated in section 3.4. These estimates are based on bulk material properties. As such, they are not accurate for a "real" Peltier device. A realistic estimate of performance should include thin film material properties and device dimensions. The following sections detail these particulars.

4.2.1 Bi_2Te_3 Properties

The Bi_2Te_3 film used for the micro-Peltier device is deposited at a flux ratio of F[Te] / F[Bi] = 2.3. The Seebeck coefficient and electrical resistivity used in performance estimates are the average of the measured results for the F[Te] / F[Bi] = 2.3 films given in Table 3.3. These values are -177 μV / K for the Seebeck coefficient and 1056 μΩcm for the electrical resistivity. The thermal conductivity for n-type Bi_2Te_3 is taken from Table 2.2 and is 0.019 W / cm°C.

4.2.2 Thin Film Gold Properties

0.15 μm thick sputtered gold films are used for the micro-Peltier device. Table 3.5 shows these films to possess a resistivity of 5 μΩcm. This value is 2.1 times greater than that of bulk gold (see Table 2.2).

The thermal conductivity of bulk gold is 3.15 W/cm°C (see Table 2.2). Since the thermal conductivity of gold is primarily due to electron conduction, it can be estimated that the thermal conductivity of thin film gold vs. bulk gold will follow the inverse ratio as that for electrical resistivity (given to be 2.1 above). Thus, the thermal conductivity of 0.15 μm thick gold films is estimated to be 1.5 W/cm°C.

The Seebeck coefficient of bulk gold is 1.94 μV/°C (see Table 2.2). This value is used for calculations and no attempt will be made to determine the true value for thin film gold. Any error due to this bulk value approximation is minimal, since Bi_2Te_3 possesses a Seebeck coefficient of significantly higher magnitude.

4.2.3 Adhesion Metal Properties

The thickness of the films used to adhere the gold metal (chrome, nichrome, or Mo-W) is significantly less than that of the gold metal (100's of Å vs. 0.15 μm). Their electrical and thermal conductivities are also poorer than that of gold (It was shown in

section 3.8.5 that the thin chrome adhesion film possessed a resistivity greater than 50 μΩcm). The resistivities and thermal conductivities of the adhesion materials are not included in any estimation of device performance, since their effects are minimal.

It is assumed that there will be no change in the Seebeck coefficient of the gold metal due to the presence of the adhesion materials. This assumption is based on the higher electrical conductivity of gold. Gold's higher conductivity will electrically short out the Seebeck voltages generated in the adhesion materials. Any error due to this approximation is minimal, since Bi_2Te_3 possesses a Seebeck coefficient of significantly higher magnitude than that of either gold or the adhesions metals.

4.2.4 PECVD SiO_2 Thermal Conductivity

The thermal conductivities of the PECVD SiO_2 films used in the construction of the micro-Peltier device were not measured. A value of 0.014 W / cmK [28] is used in the performance estimates.

4.2.5 Per Square Properties

In order to simplify the design optimization, the elements of the micro-Peltier device are divided into square regions. The thermal conductivity and electrical resistance of these regions are then calculated on a per square basis. The per square thermal conductivity (K_{sq}) and electrical resistance (R_{sq}) are calculated using,

$$R_{sq} = \frac{\rho}{t} \quad \text{ohms / square} \tag{4.1}$$

$$K_{sq} = \kappa t \quad \text{watts / square} \tag{4.2}$$

where R_{sq} is the resistance per square, K_{sq} is its thermal conductance per square, and t is the thickness of the material. Results of these calculations are shown in Table 4.1.

Table 4.1: The per square thermal conductivity (K_{sq}) and electrical resistance (R_{sq}) of the various materials of the micro-Peltier device.

Material	Thickness (μm)	R_{sq} (Ω / sq.)	K_{sq} (μW / sq.)
Gold	0.15	0.33	23
Bi_2Te_3	1.1	10	2.1
SiO_2 (fuzed quartz)	1.8	insulating	2.5

4.2.6 Specific Heat And Density

Knowledge of the specific heat and density of the materials making up the micro-Peltier pump is needed in order to estimate its thermal response time. The specific heat and density of the materials making up the micro-Peltier pump are shown in Table 4.2.

References providing this information for PECVD SiO_2 and Bi_2Te_3 were not found, however. For PECVD SiO_2, the properties of fuzed quartz are selected in its place. For Bi_2Te_3, an estimate of its properties is given using the weighted average of the bismuth and tellurium atoms making up Bi_2Te_3. The accuracy of this estimate was not investigated.[1]

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[1] In the case of specific heat, Kopp's law states that for solids the molar heat capacity of a compound at room temperature and pressure approximately equals the sum of the heat capacities of the elements in the compound [79]. Errors are considerable, particularly for lighter elements.

Table 4.2: Room temperature specific heats and densities of materials used in the fabrication of the micro-Peltier pump. Data is taken from [80].

Material	Specific Heat (J / g°C)	Density (g / cm^3)
Gold	0.13	19.32
SiO_2 (fuzed quartz)	0.75	2.2
Bismuth	0.13	9.75
Tellurium	0.21	6.24
2 Bi : 3 Te weighted average	0.18	7.6

4.3 Simulation Of A Micro-Peltier Device

The micro-Peltier device shown in Figure 1.3 is modeled in this section. This device is fabricated on a SiO_2 microbridge measuring 570 x 270 μm. The gold metal forms wire contacts for the micro-Peltier device and the thermocouple (see Figure 4.1). The various segments of the gold metal are labeled A through F. The two Bi_2Te_3 regions are labeled G and H. The gold segments A and B contact both ends of the Bi_2Te_3 film segment G forming the micro-Peltier pump. The gold segments C and D contact both ends of the Bi_2Te_3 film segment H forming the thermocouple. The gold segments E and F are wires contacting B and C to the wire bonding pads.

4.3.1 Device Model

The micro-Peltier device of Figure 1.3 is constructed on a SiO_2 microbridge with essentially a one-dimensional shape. This shape allows the use of a one-dimensional thermal conduction model to represent this device.[2] In this model, the bulk silicon wafer

[2] Thermal convection and radiation losses are ignored in this model. More will be said on convection and radiation losses in section 4.3.4.

on either side of the SiO_2 microbridge is considered an infinite thermal reservoir of stable temperature. Therefore, components which extend off the microbridge (segments E, F, and H) are considered to end at the silicon wafer when calculating Joule heating and thermal conduction losses within these components.

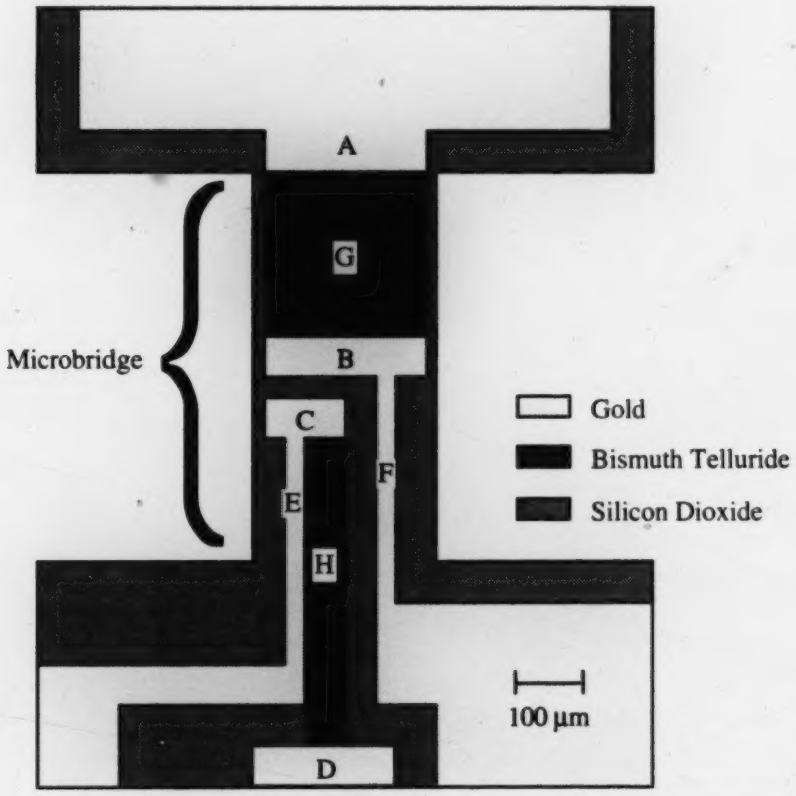

Figure 4.1: Schematic of the micro-Peltier pump of Figure 1.3.

The gold - Bi_2Te_3 junction at segment B (see Figure 4.1) is the location where the Peltier device absorbs/releases energy on the SiO_2 microbridge. The gold and Bi_2Te_3 regions of segments E to H are thermal conduction paths to the bulk silicon thermal

reservoir. The entire area of segment B is considered a uniform temperature due to the high thermal conductivity of the gold metal. Above segment B (between segments A and B), the SiO_2 (of the microbridge and the gold passivation film) is a thermal conduction path to the thermal reservoir.

Below segment B, a simplification to the model is made. It is assumed that segment C and the SiO_2 between segments B and C is at the uniform temperature of segment B. Therefore, at the bottom of the microbridge, the SiO_2 between segment C and the wafer is the thermal conduction path to the thermal reservoir. The error due to this simplification is not that significant. Looking forward to Tables 4.3 and 4.4, we see that the thermal conduction through the SiO_2 at the bottom of the microbridge is not a significant percentage of the total (3.8 μW / °C vs. 15.8 W / °C). If the above simplification were not made, the 3.8 μW / °C thermal conduction loss would be reduced by about $^2/_3$ and the total thermal loss would be reduced only around 10 %.

4.3.2 Design Optimization - Using Multiple Iterations

This section discusses the design and expected performance of the micro-Peltier device of Figure 1.3. This discussion is based on an operational temperature of 22 °C, or approximately 295 K.[3]

Maximum Cooling Power:

The first step of the design process is to select a desired pumping power (Q_{max_0}) for the Peltier device. A $Q_{max_0} = -100\ \mu W$ was selected.

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[3] The operational temperature will change as the Peltier device pumps heat, and so the selection of a fixed operational temperature is not accurate. However, the temperature differential produced by the micro-Peltier device is small with respect to room temperature (less than 10 K vs. 295 K) and so any error is small.

Electrical Resistance And Current:

With Q_{max_0} selected, the electrical resistance and operating current of the Peltier device can now be found. Using Equation 2.34 the resistance is 13.9 Ω. The operating current at Q_{max_0} is found using Equation 2.18 and is 3.8 mA.[4]

Optimized Device Dimensions:

The dimensions of the various elements of the micro-Peltier pump must now be chosen such that its electrical resistance is 13.9 Ω, while minimizing thermal conductivity losses. After several iterations, the component dimensions were selected. These dimensions are shown in Table 4.3. The resistance and thermal conductivity of each component are shown in Table 4.4.

The total device resistance is 13 Ω. This is slightly lower than desired. The extra effort needed to iterate to exactly a 13.9 Ω solution was felt unnecessary, partly due to uncertainties in the deposited material properties. It was also felt better to err towards less resistance in case contact resistance problems existed in the fabricated device. Re-calculating the cooling power for the 13 Ω resistance, we obtain a Q_{max_0} = -107 μW.

Maximum Temperature Differential:

The Peltier device has a Q_{max_0} = -107 μW and a total thermal conductivity of 15.8 μW / cmK (see Table 4.4). Using Equation 2.17 we find that this device should be capable of a maximum temperature differential (ΔT_{max}) of 6.8 °C.

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[4] It is worth noting that the Joule heating loss (the middle term on the right hand side of Equation 2.17) equals 100 μW. The gross cooling pumping power of the Peltier device is -200 μW (see Equation 2.6). Thus, the selected cooling power of -100 μW is the maximum net cooling power of the Peltier device, not considering thermal conduction losses.

Table 4.3: The dimensions of the various components of the micro-Peltier device. Lengths and widths are measured from top to bottom and from side to side respectively of Figure 4.1.

Material	Component	Length (μm)	Width (μm)	Thickness (μm)
Gold	Segment B	60	240	
	Segment C	60	120	
	Segment E on the microbridge	180	30	
	Segment F on the microbridge	270	30	
Bi_2Te_3	Segment G	240	240	1.1
	Segment H on the microbridge	180	60	1.1
SiO_2	Microbridge from A to B	240	270	1.8
	Microbridge from C to wafer	180	270	1.8

Table 4.4: Optimized component dimensions for the micro-Peltier device. The electrical resistance of the thermocouple is not considered as there is negligible current flow in this device.

Component	Resistance (Ω)	Thermal Conductivity (μW / °C)
Segment E on the microbridge		3.8
Segment F on the microbridge	3.0	2.6
Segment G	10	2.1
Segment H on the microbridge		0.7
SiO_2 microbridge from A to B		2.8
SiO_2 microbridge from C to wafer		3.8
Total:	13	15.8

Thermal Mass:

The thermal mass of this device is found by summing the individual thermal masses of all its components. The thermal mass of a component is the product of its specific heat and mass. Using the component dimensions given in Table 4.3 and specific heat and density data of Table 4.2, the thermal mass is calculated to be 0.57 μJ / °C.[5]

Thermal Response Time:

As a first order approximation, the thermal response speed from $\Delta T = 0$ °C can be found by dividing the thermal mass (0.57 μJ / °C) by Q_{max_0} (-107 μW). A slightly more accurate approximation would be to use ½ the thermal mass (0.285 μJ / °C), since we are interested in the temperature change at the center of the SiO_2 microbridge. Doing this one obtains a thermal response time of 2.7 ms / °C. It is emphasized that this is a simple approximation. A more accurate estimate should include the relative location of the components to each other and their thermal conduction losses.

Equality Of Losses At Q_{max_0}:

At ΔT_{max} the net heat pumping power (Q_{max} as given in Equation 2.19) equals zero. Equation 2.19 shows that at ΔT_{max} the thermal conduction loss (Q_T) is equal in magnitude to Q_{max_0}. Footnote 3 showed the Joule heating loss (Q_J) to also be equal in magnitude to Q_{max_0}. The equality of Q_T and Q_J at Q_{max_0} is not a coincidence. It reflects the fact that maximum performance occurs when the Joule heating and thermal losses are equal.

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[5] The removed mass of the SiO_2 passivation at the via contacts over segments B and C is ignored in this calculation.

4.3.3 Design Optimization - Mathematical Solution

Section 4.3.2 used multiple iterations to optimize the dimensions of the micro-Peltier device. Component dimensions can also be designed using Equation 2.28. This section compares the optimized design found by these two techniques.

Equation 2.28 determines the optimal dimensional ratio (γ_A/γ_B) for the simple two-junction Peltier device of Figure 2.9. For the device of Figure 1.3, γ_A is the dimensional ratio for the Bi_2Te_3 film segment G. γ_B is the dimensional ratio for the gold metal segment F. Expanding Equation 2.28 for the micro-Peltier device we have,

$$\frac{\gamma_A}{\gamma_B} = \frac{\dfrac{W_A t_A}{L_A}}{\dfrac{W_B t_B}{L_B}} = \sqrt{\frac{\kappa_B \rho_A}{\kappa_A \rho_B}} \qquad (4.3)$$

where A and B are the Bi_2Te_3 and gold films respectively, W is the segment width, t is the segment thickness, and L is the segment length. By substituting material parameters (κ_A, κ_B, ρ_A, ρ_B), and selecting the dimension for segment G (240 x 240 µm) and film thicknesses (see Table 4.3), the width and length ratio of the gold segment F can be optimized. Solving we get $W_B/L_B = 0.057$. Substituting the length of segment F (270 µm), we find that the its width should be 15.4 µm.

The final width found in the optimization of section 4.3.2 was 30 µm. This is approximately double the optimal design of 15.4 µm given by Equation 4.3. In order to compare the two solutions, Q_{max_0} and ΔT_{max} is calculated for the width 15.4 µm.

Electrical Resistance And Current:

The resistance of segment F is now 5.8 Ω, yielding a total device resistance of 15.8 Ω.

Maximum Cooling Power:

Equation 2.34 gives Q_{max_0} = -88 μW. The solution of section 4.3.2 showed Q_{max_0} = -107 μW.

Maximum Temperature Differential:

The thermal conductivity of segment F on the microbridge is 1.3 μW / °C, yielding a total thermal conductivity of 14.5 μW / °C. Equation 2.19 gives ΔT_{max} = 6.1 °C. The solution of section 4.3.2 showed ΔT_{max} = 6.8 °C. The closeness of these two solutions indicates that the optimization of section 4.3.2 is a good one.

Comparison Of The Two Solutions:

It is worth asking why the solution given by Equation 4.3 yields a slightly poorer performing device than that found in section 4.3.2 (6.1 °C vs. 6.8 °C). The reason is that Equation 4.3 does not fully reflect the complexity of the micro-Peltier device. It does not include the presence of the temperature sensing thermocouple and the SiO_2 microbridge. In order to obtain an accurate result, Equation 4.3 would have to be modified to include these elements. However, this was not deemed to be worthwhile, since the solution found in section 4.3.2 is very close to that of Equation 4.3.

4.3.4 Thermal Convection And Radiation Losses

Thermal convection losses will not be discussed. This is because maximum performance testing for the micro-Peltier pump was conducted in a vacuum environment. Thermal radiation losses are discussed briefly below.

Thermal radiation from a surface is calculated using Equation 2.35, shown again below.

$$Q_r = \varepsilon\sigma\left(T_s^4 - T_o^4\right) \quad W/m^2 \qquad (2.35)$$

As an approximation, assume the entire surface of the micro-Peltier device is at a uniform temperature and that it has an emissivity of $\varepsilon = 1$. The surface area of the micro-Peltier device is 570 x 270 = 154 nm^2. Let us assume it is at the maximum temperature reduction of 6.8 °C and that the surroundings are at 295 K. Equation 2.35 gives us a thermal radiation of 5.9 μW. The total thermal radiation is twice this value, 11.8 μW, since energy will radiate from both the top and bottom of the micro-Peltier device.

Section 4.3.2 showed the total thermal conductivity losses at ΔT_{max} to be 107 μW. This value is 9 times the estimated radiation losses. Thus, the exclusion of thermal radiation from the device model does not cause significant error.

4.4 Performance Of A Micro-Peltier Device

The micro-Peltier device (shown in Figure 1.3) was fabricated using Cr-Au-Cr metallization and a 1.1 μm thick Bi_2Te_3 thin film. The Bi_2Te_3 film was deposited at F[Te]/F[Bi] = 2.3, possesses a resistivity of 1150 μΩcm, and a Seebeck coefficient of -187 μV / K. This device is not passivated by a SiO_2 layer as described in section 3.9.2.

Joule Heating Problems:

The device of Figure 1.3 has a total electrical resistance of 52.9 Ω. This is much higher than the predicted resistance of 13 Ω shown in Table 4.4. The higher resistance is due to chrome inter-diffusing with the gold metal during the elevated temperatures of the PECVD SiO_2 process and the Bi_2Te_3 deposition (see section 3.8.6). The result of the increased device resistance is a significant loss of device performance (in both Q_{max_0} and ΔT_{max}) due to excessive Joule heating.

Maximum Cooling Power:

The maximum cooling is found to occur at 1.03 mA. Equation 2.34 gives Q_{max_0} to be -29 μW. This value is significantly lower than that predicted in section 4.3.2 due to the above mentioned Joule heating problem.

Current-Voltage Relationship:

Current-voltage measurements show the Bi_2Te_3 - gold contact to be ohmic in nature (See Figure 4.2).

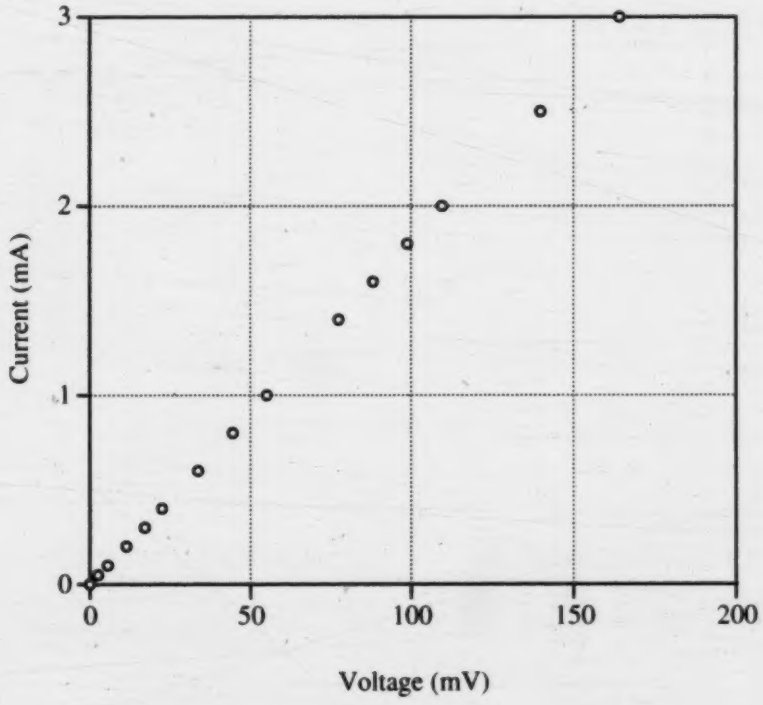

Figure 4.2: Current-voltage relationship of the micro-Peltier device. The straight line nature of the data suggests the Bi_2Te_3 - gold contact is ohmic.

Maximum Temperature Differential:

A plot of temperature differential vs. pumping current is shown in Figure 4.3. Two temperature differentials are shown. One is for the Peltier device operating in air, and the other is for operation at a pressure of 50 mTorr.[6] Maximum temperature reductions (ΔT_{max}) of 0.30 °C in air and 1.5 °C at 50 mTorr are observed.

The large difference in these values clearly indicates that thermal convection plays a significant part in thermal losses at atmospheric pressure.

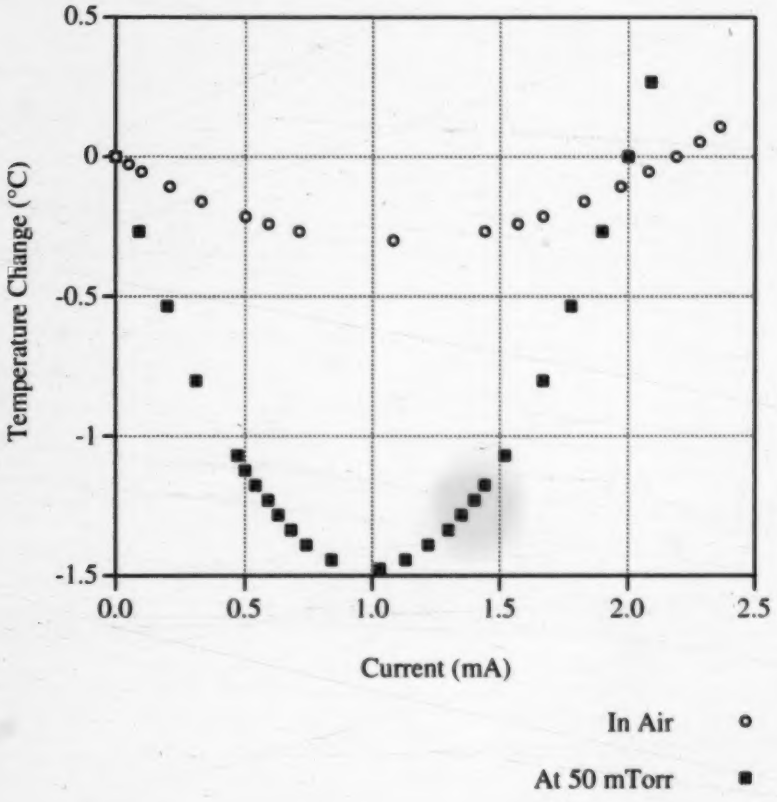

Figure 4.3: Temperature reduction vs. device current.

[6] Measurements at lower pressures showed no further improvement in ΔT_{max}.

Thermal Response Time:

Figure 4.4 shows the thermal response time of the Peltier device at a pressure of 50 mTorr. The upper curve is an applied current pulse (1.03 mA) to achieve Q_{max_0} for 50 ms, and the lower curve is the thermal response of the heat pump. It can be seen that the initial cooling rate of the Peltier device is 8.3 ms / °C, and the initial thermal relaxation rate is 7.6 ms / °C.[7]

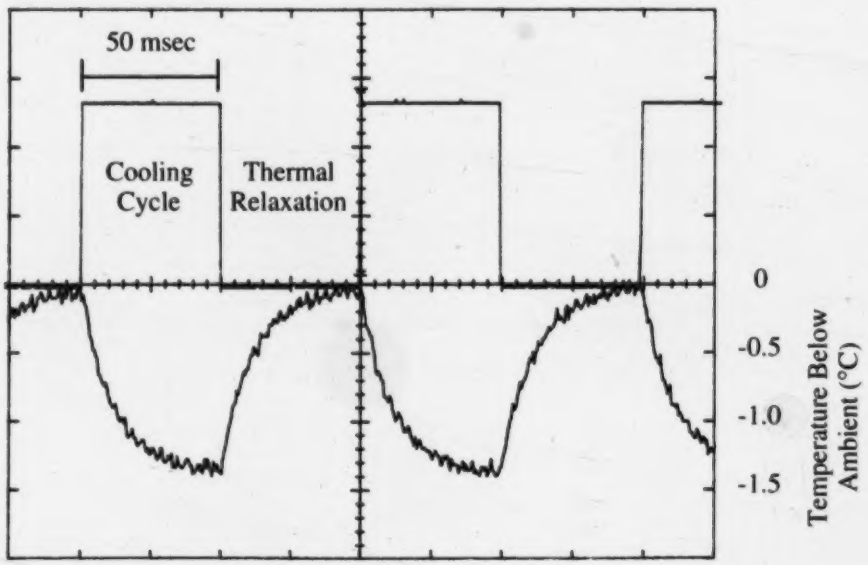

Figure 4.4: Thermal response time at a pressure of 50 mtorr.

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[7] The thermal relaxation time could be significantly decreased by running the Peltier device in the heating mode.

4.4.1 Other Discussions

Further discussions of the fabricated micro-Peltier device and comparisons with the device model in section 4.3.2 are given below.

Presence Of The SiO_2 diaphragm:

It was mentioned in section 3.8.7 that the SiO_2 microbridge was not initially re-patterned in process step 13 (see section 3.7), leaving a 0.3 μm thick SiO_2 diaphragm surrounding the microbridge. The performance of the Peltier device was measured before and after RIE of the SiO_2 diaphragm. It was found that the SiO_2 diaphragm decreased the performance of the Peltier device by 9 %. This analysis was done at atmospheric pressure.

Thermal Conductivity Comparison:

The predicted thermal conductivity for this Peltier device was 15.8 μW / °C (see Table 4.4). The measured ΔT_{max} of 1.5 °C at 50 mTorr and Q_{max_0} of -29 μW indicates that the true thermal conductivity is 19.3 μW / °C. Thus, the predicted thermal conductivity is realistic.

Thermal Response Time Comparison:

Using the simple approximation shown in section 4.3.2, the initial cooling rate of a Peltier device with Q_{max_0} of -29 μW and a thermal mass of 0.57 μJ / °C would be 9.8 ms / °C. This is very close to the measured value of 8.3 ms / °C, indicating that the approximation of section 4.3.2 is reasonable.

4.5 Performance Of Other Devices

Performance results for two other micro-Peltier devices are given in this section. These devices were fabricated in the same batch as the above device, but possess different dimensions. The dimensions of the devices are shown in Table 4.5.

The wider device possesses a resistance of 32.5 Ω and a Q_{max_0} of -47 μW. The thinner device possesses a resistance of 46.9 Ω and a Q_{max_0} of -32 μW. Plots of temperature differential vs. pumping current for these devices are shown in Figure 4.5. The wider device achieves a ΔT_{max} of 0.43 °C in air and 1.5 °C at 50 mTorr. The thinner device achieves a ΔT_{max} of 0.33 °C in air. Thermal response times for these devices were not measured. However, they are expected to possess slightly faster response times to the device of section 4.4, due to their smaller thermal masses with respect to cooling power.

Table 4.5: The dimensions of the various components of two micro-Peltier devices.

Material	Component	Dimensions (Length x Width in μm)	
		Wide Device	Thin Device
Gold	Segment B	60 x 330	60 x 180
	Segment C	60 x 120	60 x 90
	Segment E on the microbridge	150 x 30	150 x 30
	Segment F on the microbridge	240 x 60	240 x 30
Bi_2Te_3	Segment G	120 x 330	120 x 180
	Segment H on the microbridge	150 x 60	150 x 60
SiO_2	Microbridge	420 x 360	420 x 210
	Microbridge from A to B	120 x 360	120 x 210
	Microbridge from C to wafer	150 x 360	150 x 210

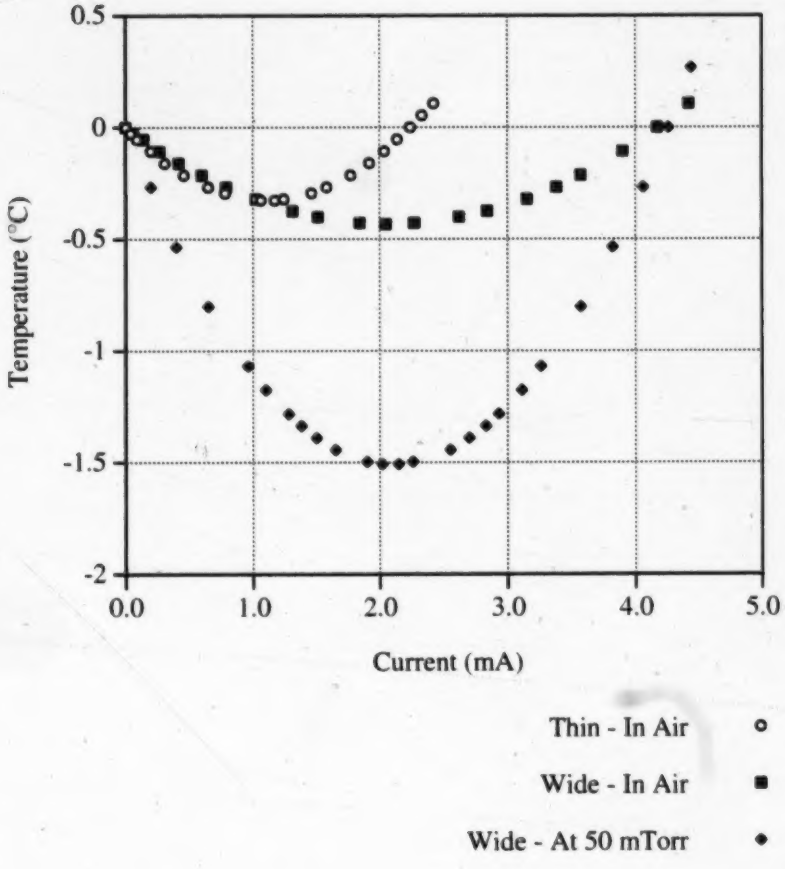

Figure 4.5: Temperature reduction vs. device current for two Peltier devices.

4.6 Devices Using Mo-W Adhesion Material

Devices using Mo-W as the adhesion material will not possess the Joule heating problems of the above fabricated devices, and so they should perform closer to that of the device model of section 4.3.2. However, Bi_2Te_3 adhesion problems due to organic contamination (see section 3.8.1) prevented the completion of the Mo-W devices. Development of these devices is on-going, however, and hopefully they will be completed soon after the writing of this thesis.

4.7 Larger And Smaller Devices

As indicated in Equation 2.34, the heat pumping power (Q_{max_0}) of a Peltier device is inversely proportional to its electrical resistance. It is worth noting that smaller scale devices can achieve the same heat pumping rate as larger scale devices as long as the resistance is the same. For example, a Peltier pump measuring both 10 times shorter and narrower than another would possess the same heat pumping rate, since both devices possess the same electrical resistance. Furthermore, both devices would also possess similar ΔT_{max}, as the thermal conductivity increases inversely proportionally with the electrical resistance (see Equations 2.21 and 2.22).

Smaller devices would, however, have the advantage of lower thermal radiation and convection losses through the surrounding air (These losses increase with increasing surface area [53].). Therefore, their ΔT_{max} would be higher than that of larger devices of the same cooling power.

4.8 Thicker Gold And Bi_2Te_3 Thin Films

It is mentioned above that varying the scale of a device will not significantly affect its ΔT_{max}. Therefore, if one were interested in fabricating Peltier devices with larger ΔT_{max}, one would have to increase the thickness of the gold and Bi_2Te_3 thin films

with respect to the thickness of the SiO_2 microbridge. In this way, the thermal conductivity of the device will not increase as rapidly as its electrical resistance would decrease.

4.9 Ultimate Performance

The maximum ΔT_{max} possible out of a micro-Peltier device will occur when the SiO_2 microbridge and the thermocouple are infinitely small compared to the gold and Bi_2Te_3 films making up the Peltier device. That is to say, the microbridge and thermocouple would possess no thermal losses. This ultimate performing device will possess the optimized dimensions discussed in section 4.3.3, with Q_{max_0} = -88 μW and a total thermal conductivity of 3.4 μW / °C. Equation 2.19 gives a ΔT_{max} of 26 °C for this device.

We should be able to calculate the same result using Equations 2.30 and 2.33 (see section 3.4). Substituting the material properties described in section 4.2, we obtain a $z_{AB\ max}$ = 0.61 and a ΔT_{max} = 27.7 °C. This result is very close to that found above. Any discrepancy is due to round off error in the calculations of sections 4.3.2 and 4.3.3. It is worth noting that the ΔT_{max} calculated for the thin film materials (27.7 °C) is notably lower than that predicted in Table 3.2 for bulk material properties (42 °C).

4.10 Future Designs

The discussion of section 4.9 clearly shows that future device designs should concentrate on increasing the size of the Peltier device relative to the thermocouple and the SiO_2 microbridge. Referring to Table 4.4, we see that the thermocouple and the SiO_2 microbridge are responsible for ~ 30 % and ~ 40 % respectively of the thermal conduction losses. The thermocouple dimensions should be reduced greatly[8] or it should be replaced

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[8] This would require the purchase of higher quality photolithography masks than the linotronic printed masks used for this thesis.

altogether by another temperature sensing mechanism. The relative size of the SiO_2 microbridge should be made smaller by using thinner SiO_2 films or thicker Bi_2Te_3 films.

As an example, let us ignore the thermocouple and assume the gold and Bi_2Te_3 thin films are increased in thickness five times (An ~ 5 μm thick Bi_2Te_3 is not unreasonable.). Such a device will have five times the cooling power of the ultimate device described in section 4.9. It will have a Q_{max_0} = -440 μW and a total thermal conductivity of ~ 24 μW / °C. Equation 2.19 gives a ΔT_{max} of ~ 18 °C for this device. Using the method described in section 4.3.2, the thermal mass of this device will be ~ 0.90 μJ / °C and the thermal response time will be ~ 2 ms / °C.

It should be noted that the above discussion is based on the simple model of section 4.3.1.

4.11 Replacing The Gold Metal With p-Type Sb_2Te_3

Let us briefly consider what will happen if the gold metal is replaced with p-type Sb_2Te_3 (p-type Sb_2Te_3 was not considered for the micro-Peltier device due to its toxic properties, as explained in section 3.4.). Referring to Table 2.2, and Equations 2.31 and 2.34 we see that for the device of section 4.10, Q_{max_0} will triple to -1.32 mW and ΔT_{max} will increase 1.5 times to ~ 27 °C.

Chapter 5

STRUCTURE AND PROPOSED APPLICATIONS OF MICRO-PELTIER DEVICES

"Gyroscope, n.:

A wheel or disk mounted to spin rapidly about an axis and also free to rotate about one or both of two axes perpendicular to each other and the axis of spin so that a rotation of one of the two mutually perpendicular axes results from application of torque to the other when the wheel is spinning and so that the entire apparatus offers considerable opposition depending on the angular momentum to any torque that would change the direction of the axis of spin."

-- Webster's Seventh New Collegiate Dictionary

5.1 Introduction

This chapter will briefly discuss series and multi-staged Peltier devices. These geometries provide increased performance over that of single stage Peltier devices. Following this, numerous applications where the micro-Peltier device could prove useful are presented. A discussion on the fabrication of thermally isolated circuits on microstructures is given at the end of this chapter.

5.2 Series And Multi-Stage Peltier Devices

Peltier devices are often connected in series or stacked in multiple stages in order to achieve greater performance. This section briefly introduces the reader to these device

geometries.

5.2.1 Series Devices

The problem with using a single Peltier device to thermally control a region, is that there is only one location where heat conduction actively takes place (see Junction 1 in Figure 2.9). This is unacceptable in situations where uniform heat pumping is required. Fabricating multiple Peltier devices spaced evenly in contact with the region provides more uniform heat pumping. This is illustrated in Figure 5.1.

The Peltier devices of Figure 5.1 are electrically connected in series, but thermally in parallel. More uniform heat pumping is provided to the thermally controlled region, and only one power supply is required. Fabricating multiple series micro-Peltier devices would require precise lithographic control.

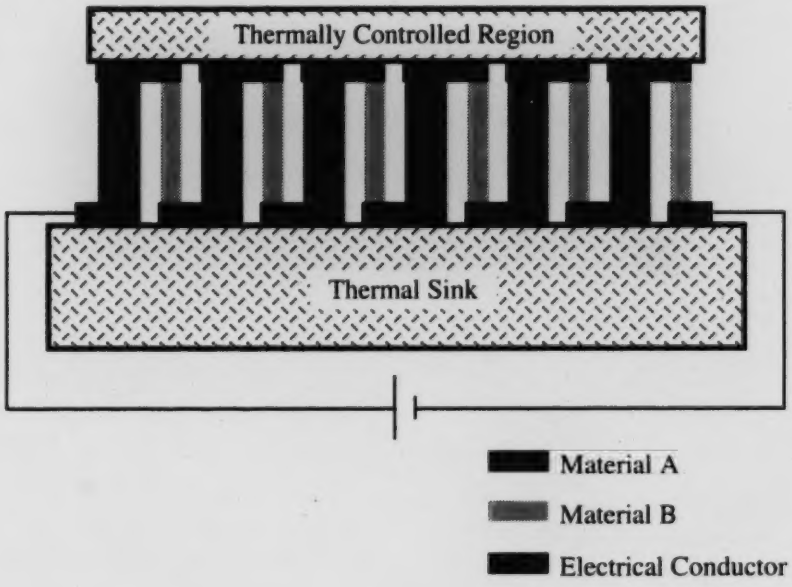

Figure 5.1: Multiple Peltier devices connected to a thermally controlled region.

5.2.2 Multi-Stage Devices

The temperature differential achievable by a single Peltier device is a function of its geometry and material composition (see section 2.5.3), and so it cannot be increased beyond a maximum (ΔT_{max}). However, one can achieve higher temperature differentials by stacking Peltier devices, forming a multi-stage device [17,44,54].

A two-stage Peltier stack is shown in Figure 5.2, where the individual ΔT_{max} for two Peltier devices are added together, thereby achieving a maximum temperature differential of $\Delta T_{max\ Total} = \Delta T_{max\ 1} + \Delta T_{max\ 2}$.

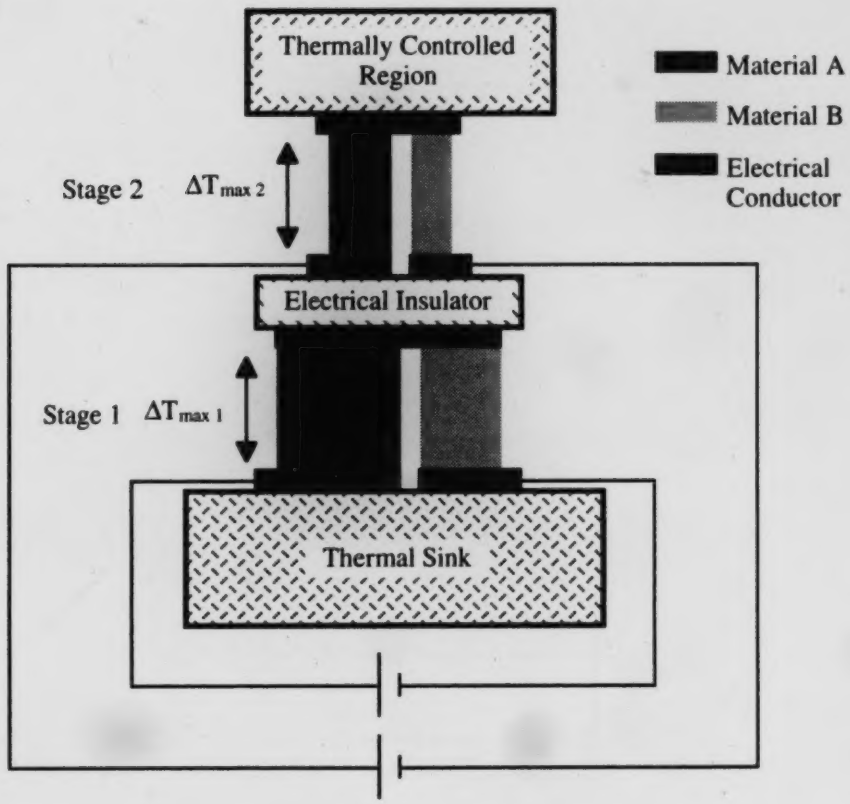

Figure 5.2: A two-state Peltier device.

Figure 5.3 shows a second example, where the stacked geometry is such that only a single power supply is required. This geometry is preferred for two-stage devices, because the lack of wiring to the second stage reduces thermal conduction losses.

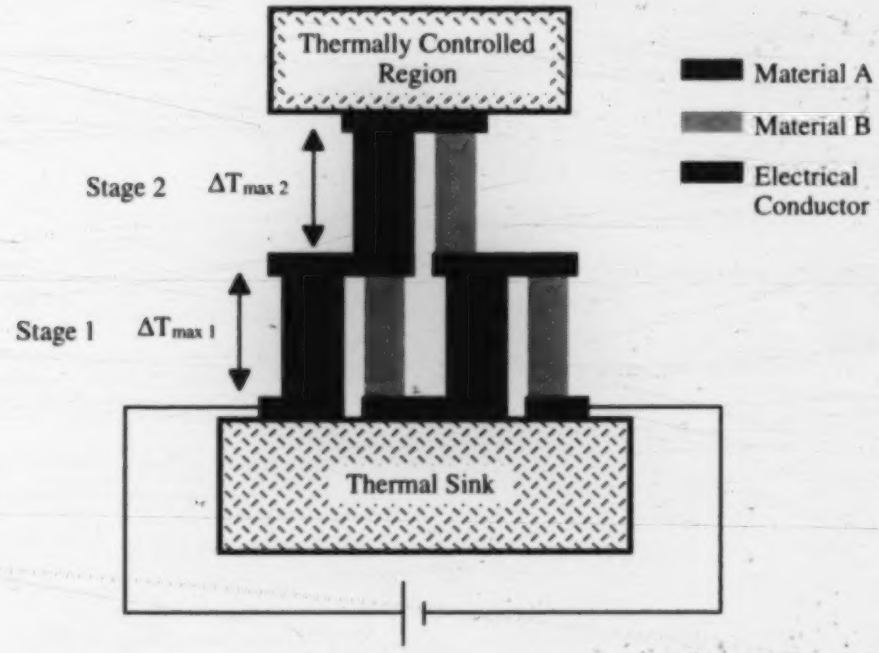

Figure 5.3: Two-stage Peltier device using a single power supply.

It is important to note that the stages lower in the stack (closer to the thermal sink) must possess increasing heat pumping capability. This is because each lower stage must remove the combined thermal energy pumped by the stages above it.

There is a limit to how large a temperature reduction can be achieved between the top and bottom of a Peltier stack. This limit is reached because a material's Seebeck coefficient, electrical and thermal conductivities are temperature dependent. As the temperature is reduced, a point is eventually reached where the efficiency of the coldest

Peltier stages reaches zero.

The best single-stage bismuth telluride Peltier devices (using both n and p-type Bi_2Te_3) can achieve temperature drops of 70 °C below room temperature. Two-stage stacked devices can achieve temperature drops of over 100 °C. An experimental eight-stage device, the coldest three of which make use of bismuth antimony alloys, has achieved a temperature drop of 171 °C below room temperature [20].

5.3 Applications For The Micro-Peltier Device

The performance of micro-Peltier devices was discussed in Chapter 4. With the thin film materials used, section 4.10 showed that a $\Delta T_{max} \sim 18$ °C with a thermal response time of ~ 2 ms / °C is not unreasonable.

One or more micro-Peltier pumps fabricated within a single IC (or other device) will allow for precise and rapid localized thermal control of components within the IC. Thermal control can be used to compensate for fluctuations in the ambient temperature, or to thermally "tune" select devices. Micro-Peltier pumps can also be used in conjunction with exterior (outside the IC package) heat pumps, forming a two-stage thermal control system. Such a scheme would be useful when bulk IC thermal control is needed in addition to rapid on-chip thermal control.

Section 1.3 detailed the benefits of using micro-Peltier devices over the existing thermal control technology of resistive micro-heaters. Briefly, these benefits are:

- A decreased thermal relaxation time for thermally isolated microstructures.
- The possibility of a microstructure to exist at a temperature below ambient.
- A power saving over existing techniques of IC die or package cooling.

Several applications where the implementation of one or more micro-Peltier devices can be of benefit are presented in the following sections.

5.3.1 Thermal Modification Of Resistance

On-chip Peltier devices can be used to thermally adjust the electrical resistance of thin film materials. Such control allows:

- The tuning of thin film resistors.
- Gain control for on-chip amplifiers by varying input or feedback resistors.
- Gain and cut-off frequency control for on-chip RC, RL, or RLC filters.
- Micro-Peltier devices, used to enhance an exterior cooling system, could be used to switch high temperature superconducting devices "on" or "off."

The amount of resistance variation depends on the temperature coefficient of resistivity of the material in question. The small temperature variations achievable by single stage micro-Peltier devices will not greatly affect the resistance of metals[1] (Small resistive variations will still be important in high precision circuitry.[2]). The resistivity of semiconductors, on the other hand, is proportional to carrier concentration which can be exponentially dependent on temperature[3] (This topic will not be discussed here and readers are directed to [31,55] for details.).

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1 For example, the temperature coefficient of resistivity of Aluminum is 0.00429 % per degree Kelvin at room temperature [80].

2 A personal visit to the institute of standards in Australia (summer 1989) revealed that in some cases electronic equipment is turned on for two days prior to high precision measurements, in order for the equipment to thermally stabilize.

3 The intrinsic carrier concentration doubles every 11 °C for silicon [31].

5.3.2 Thermal Modification Of Dielectric Constant

The dielectric constant of a material can be controlled thermally. Examples of possible uses are:

- The tuning of the transmission or reflection coefficients of a thin film.
- The degree of polarization rotation within a film can be varied.
- The modification of the speed of propagation within a thin film.

The thermal modification of propagation speed is currently used in a commercial fiber optic switch sold by IONAS. This "thermo-optic switch" consists of two microfabricated fiber optic lines and a gold thin film heater attached to one of the lines [56] (see Figure 5.4). Turning on the heater increases the refractive index of the fiber under it. By controlling the power, and thereby the phase difference between the light in the two fibers, the switch is able to select the output port. The heater requires 0.6 W and has a response time faster than 0.5 ms.

Replacing the heater with a micro-Peltier pump would enable the speeding up, slowing down, or stabilization of signal propagation speed [52].

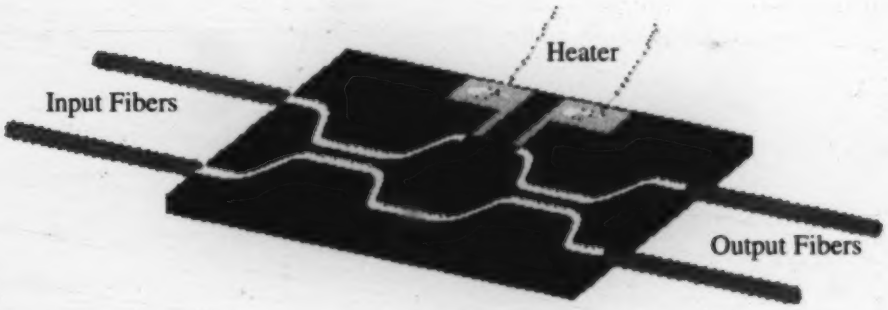

Figure 5.4: A thermo-optic switch fabricated by IONAS [56].

5.3.3 Thermal Tuning Of Semiconductor Junctions

The current-voltage (I-V) relationship of many semiconductor devices is highly temperature dependent. For example, the forward and reverse currents of a pn junction (given by Equation 5.1 and 5.2) increase exponentially with temperature [31].

Forward Current[4] $$J_F \sim e^{-\frac{(E_g - qV)}{kT}} \quad A/cm^2 \qquad (5.1)$$

Reverse Current $$|J_R| \sim e^{-\frac{E_g}{kT}} \quad A/cm^2 \qquad (5.2)$$

where E_g is the semiconductor bandgap, q is the electron charge, V is the junction bias voltage, k is Boltzmann's constant, and T is the temperature in Kelvin. On-chip Peltier devices can be used for:

- The thermal tuning of the I-V characteristic of a semiconductor device.
- The thermal stabilization of the I-V characteristic of a semiconductor device over a variety of current loads. Normally, a change in current load would result in changes in Joule heating and so the operation temperature.
- The temperature regulation of a bandgap voltage reference.

A thermally isolated bandgap voltage reference has been fabricated on a cantilevered SiO_2 suspension platform [57,58]. This device uses micro-heaters to thermally regulate

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[4] It is worth noting that the forward bias current is typically approximated in textbooks as,

$$J_F \sim J_s e^{\frac{qV}{kT}} \quad A/cm^2 \qquad (5.3)$$

where J_s is the reverse saturation current. Equation 5.3 seems to indicate that J_F decreases with increasing temperature. This assumption is, however, incorrect. Substitution of the full J_s term reveals the form as shown in Equation 5.1.

the bandgap reference. The thermal time constant is 2.5 ms, which is two orders of magnitude faster than previous heater controlled voltage references. Implementation of a micro-Peltier device would have the benefit of two-way temperature stabilization.

5.3.4 Thermal Control For Laser Diodes

Integrating a micro-Peltier pump with a semiconductor laser diode provides several benefits. Examples are:

- The thermal stabilization of output power. As the temperature of a diode laser rises, its output power decreases. This is due to a reduction in the number of electrons in the population inversion state, caused by a change in the Boltzmann population distribution of the electrons [59].

- An increase in laser lifetime. In general, the operating life doubles with every 10 °C reduction in temperature, and conversely halves with every 10 °C increase [59]. Integrated Peltier devices can be used to reduce or prevent an increase in the temperature of a diode laser.

- The thermal tuning of the emission frequency of laser diodes. In laser diodes the emission frequency varies on average 0.4 nm / °C [59].

A Peltier element placed on the exterior of an 8 cm laser package has been used to adjust the output frequency of a laser diode [60]. The Peltier element varied the temperature between 5 - 41 °C, and tuned the frequency by 30 nm for a 3.5 μm laser.

Laser diodes typically consume power on the order of 10's to 100's of milliwatts. Fabricating a 10+ mW micro-Peltier device is possible. It is simply a matter of selecting device dimensions to increase heat pumping power. Also, multi-stage Peltier devices can be considered.

5.3.5 Thermo-Mechanical Driving

The micro-Peltier device can be use to modify the size of a microfabricated structure by way of thermal expansion or contraction. Some applications are:

- The micro-Peltier device can counteract stress variations in a microstructure due to a change in the ambient temperature. Alternately, stress can be induced upon a microstructure by the micro-Peltier device.

- The tuning or stabilization of resonating structures [4,13].

- The thermo-mechanical actuation of switches or pumps.

- The thermal actuation of thin film shaped memory alloys (SMA) [61]. These alloys possess up to three orders of magnitude greater actuation forces than piezoelectrics [62]. The capability to both heat and cool a SMA would allow the fabrication of bidirectional actuators.

5.3.6 Thermal Tuning Of On-Chip Sensors

Applications using thermally sensitive microsensors will benefit from on-chip thermal control. Examples are:

- The thermal stabilization of sensor characteristics.

- The reduction of measurement error and sensitivity.

Thermal based sensors (such as microsensors measuring gas-flow [1-5], temperature, radiation [4-11], and AC power [5,12,63]) use a temperature difference (ΔT) between a sensing platform and a reference as their measurement mechanism. Heat losses off the

measurement platform introduces error[5] and a sensitivity reduction to the measurement. These effects become progressively greater the higher the ΔT.

An integrated Peltier pump can be used to reduce the ΔT. The amount of energy used by the Peltier pump to reduce the ΔT will have to be factored into the sensor measurement. This can be done in software.

5.3.7 Thermal Control Of Chemical Or Biological Reactions

Reaction rates depend on both the molecular collision rate and a threshold activation energy. Experiments have shown that virtually all rate constants show an exponential increase with temperature [64]. On-chip chemical or biological reaction chambers will benefit from localized thermal control. Some benefits are:

- The thermal modification of reaction rate.
- The thermal triggering of reactions.
- The thermal stabilization of reaction rate.

5.3.8 On-Chip Micro-Calorimeters

Calorimeters are used to measure chemical and biological reaction rates [65-68]. Peltier pumps are currently used as measurement sensors in some of these calorimeters [68]. In these devices, the Peltier pump is used to compensate for a temperature difference (ΔT) between a reaction vessel and a thermal reference. The amount of energy used by the Peltier pump to reduce the ΔT is indicative of the reaction energy.

On-chip micro-calorimeters have been fabricated by several groups [69-73]. These

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[5] This error can be compensated for in software in some cases.

devices use thermopile sensors to detect the ΔT caused by a reaction within a microfabricated reaction chamber. Micro-reaction chambers require a very small volume of reactants (less than 10^{-6} moles of reactants is not uncommon, with work progressing to systems capable of measuring 10^{-12} moles of reactants). Due to the minuscule energy exchange within these micro-reaction chambers, thermally isolated reaction vessels possessing small thermal mass are required in order to achieve high measurement sensitivity. These thermally isolated chambers have the following disadvantage. When a reaction occurs, the energy released (or absorbed) will change the local temperature of the reaction vessel. Therefore, the reaction rate within the vessel will change.

On-chip micro-Peltier pumps can be used to stabilize the temperature, and so the reaction rate, within micro-reaction chambers.

In the fields of chemistry, biophysics, and biomedical engineering, Peltier pump based calorimeters allow [74]:

- The measurement of reaction rates of endothermic or exothermic reactions. This can be used for measurements of bonding energy or binding energy (such as proteins binding to cells or enzymes).

- The in-situ thermal modification or stabilization of reaction rates.

- The measurement of energy exchange during cell division or other life processes.

- The transparent nature of the SiO_2 thermal isolation microbridge allows for optical measurements during the calorimeter measurements.

Fabricating micro-fluidic channels on the micro-Peltier device would not significantly affect its performance. For example, a 5.5 nanomole reaction chamber[6] is

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[6] At standard pressure and temperature, water has a molecular density of 0.055 mol / ml. A micro-reaction chamber measuring 100 x 100 x 10 µm, for example, would fit on the SiO_2 microbridge and possesses a volume of 100 picolitres and holds 5.5 nanomoles of fluid.

fed by two channels measuring 100 μm long, 20 μm wide, and 10 μm deep[7] on the SiO_2 microbridge. Assume water is the fluid medium.[8] Using the thermal conductivity of water of 0.0066 W / cm°C [75] and Equation 2.22, the two channels together possess a thermal conductivity of 2.64 μW / °C (assuming no fluid flow). This value is only 14 % of the measured thermal conductivity of 19.3 μW / °C for the Peltier device (see section 4.4.1). Using the specific heat of water of 4.184 J / cm^3, the thermal mass of the water in the 5.5 nanomole reaction chamber and the two fluid channels is 0.50 μJ / °C. This value is comparable to the 0.57 μJ / °C estimated for the Peltier device (see section 4.3.2).

It is worth asking how much energy is released in a nanomole reaction. Table 5.1 lists the enthalpy change for some enzyme-catalyzed reactions. These energies are within the Q_{max_0} of the micro-Peltier pumps described in chapter 4. Therefore, the micro-Peltier pump could be used as a micro-calorimeter for the reactions of Table 5.1.

Table 5.1: Molar enthalpy change for some enzyme-catalyzed reactions [66-68].

Enzyme	Substrate	-ΔH (kJ / mol)	-ΔH (μJ / nanomole)
Catalase	Hydrogen Peroxide	100	100
Cholesterol oxidase	Cholesterol	53	53
Glucose oxidase	Glucose	80	80
Lactate dehydrogenase	Sodium pyruvate	62	62
β-Lactamase	Penicillin G	67	67
Trypsin	Benzoyl-L-argininamide	29	29
Urease	Urea (phosphate buffer)	61	61

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[7] The width and depth of these channels are similar to those fabricated by the Alberta Microelectronic Centre.

[8] Since the heat capacity and thermal conductivity of most organic solvents is two to four times lower than that of water, a considerably higher measurement sensitivity is expected when using organic solvents as the fluid medium.

5.3.9 Other Possible Applications

In addition to the applications mentioned in the above sections, there are many other applications where a micro-Peltier pump can see use. Some are:

- The thermal modification or stabilization of the oscillation frequency of crystals.
- The thermal stabilization of piezoelectric devices. This can be of use in applications requiring high precision microfabricated actuators.
- The thermal control of an on-chip chemical potential by controlling the temperature of the reactants.

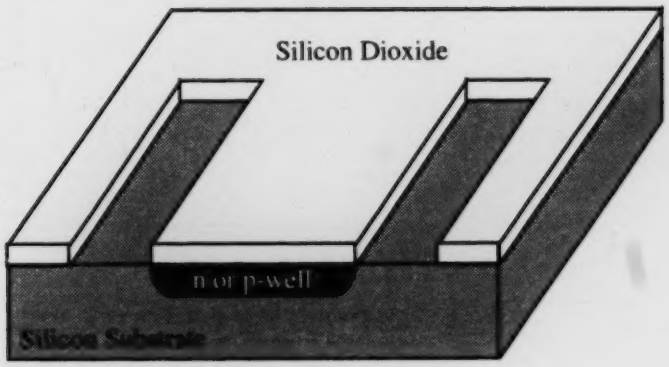
5.4 Fabrication Of Thermally Isolated Circuitry

Thermally isolated circuitry can be fabricated either below or above a dielectric platform.

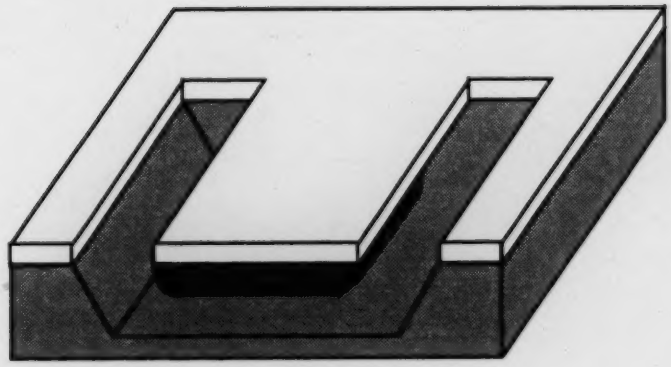
Fabricating devices below a thermal isolation platform can be done as follows. The devices are first fabricated within a doped well. They are then passivated by the dielectric which will make up the thermal isolation platform. The silicon substrate surrounding the dielectric platform is exposed (see Figure 5.5a). The silicon is then etched with the doped well biased such that it acts as an etch stop (see Figure 5.5b). This technique is readily applicable to CMOS devices which are already fabricated within doped wells. Various CMOS devices have been fabricated within n-wells below thermally isolated dielectric platforms by Kovacs et al. [57-58,63,76-77].

Fabricating devices above a thermal isolation platform requires a silicon on insulator (SOI) process (A good discussion of thin film SOI devices and processes is given in [78].). After fabrication and passivation of the SOI devices, the silicon substrate surrounding

the dielectric platform is exposed. The underlying silicon is then etched away to free the dielectric platform.



(a)



(b)

Figure 5.5: Schematic of the circuit undercutting process. (a) After completion of the device processing. (b) After release of the thermal isolation platform.

Chapter 6

SUMMARY AND RECOMMENDATIONS

"The reasonable man adapts himself to the world; the unreasonable one persists in trying to adapt the world to himself. Therefore all progress depends on the unreasonable man."

-- George Bernard Shaw

6.1 Summary

The thesis was undertaken to develop the necessary process technology to allow the fabrication of a thin film Peltier heat pump. Five key technologies were investigated.

- The fabrication of stress free SiO_2 microstructures.
- The deposition of thin film bismuth telluride by co-evaporation of bismuth and tellurium.
- The study of specific lithography and etching issues for the bismuth telluride film.
- The selection of gold metal as the secondary conductor and molybdenum-tungsten as its adhesion film.
- The study and selection of sputtered SiO_2 films as the passivation for completed micro-Peltier devices.

A sixth technology investigated in this thesis was the use of linotronic printed masks as a cost saving measure over traditional photolithographic masks.

The successful development of the above technologies resulted in the fabrication of a prototype micro-Peltier device. This device closely agreed with the performance estimates of the device model described in Chapter 4, when the problem of chrome diffusion in the gold metal is taken into consideration. The discussion of section 4.10 showed that with the thin film materials used, a ΔT_{max} ~ 18 °C with a thermal response time of ~ 2 ms / °C for the micro-Peltier device should be achievable.

6.2 Recommendations

Future device designs should concentrate on increasing the size of the Peltier device relative to the thermocouple and the SiO_2 microbridge. The thermocouple can be reduced in size or it can be replaced by another temperature sensing mechanism. The relative size of the SiO_2 microbridge can be made smaller by using thinner SiO_2 films or thicker Bi_2Te_3 films.

With the success of the sputtered SiO_2 passivation film, consideration should be given to a frontside etch technique to free the SiO_2 microbridge. Frontside etching could be done after fabrication of the micro-Peltier device. This would simplify device processing and would be more economical. The use of cantilevers should also be considered for the thermal isolation microstructure.

Consideration should also be given to the replacement of the gold metal with a p-type thermoelectric material (such as p-type Sb_2Te_3 or Bi_2Te_3). The high Seebeck coefficient of these materials would increase the performance of the micro-Peltier device.

Finally, multi-stage micro-Peltier devices should be considered. Stacking Peltier devices upon each other would increase the maximum temperature differential.

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Appendix A

PHOTO-REDUCED LINOTRONIC MASKS AND SLIDE MASKS

A.1 Introduction

In section 3.2 the use of linotronic printed masks for photolithography was discussed. Before this technique was decided upon, two other mask generation techniques were investigated. These were photo-reduction of linotronic masks and the use of photographic slides as masks. Although both of these techniques were eventually abandoned, they are described briefly below.

A.2 Photographic Reduction Of Linotronic Masks

Photographic reduction of linotronic images was tried in an attempt to generate higher resolution masks. The photographic reduction was done by University of Alberta Photographic Services. Photo-reduction of linotronic images up to 3x was performed onto both 35 mm and 4 x 5 inch Kodak Ektographic HC film. The film negatives were used as masks for the photolithography.

Kodak Ektographic HC film is a Kodalith film which develops only black or white features. It possesses a very slow speed with an ISO rating of 8. Discussions with a technical support representative of the Eastman Kodak Company lead to the choice of this film. It is the highest resolution film available from Kodak. Kodak claims this film capable of 2.5 μm feature sizes. This film is also a negative film, requiring the linotronic image to be the negative of what the photo-reduced mask is to be.

Image reductions of $^{2}/_{3}$, $^{1}/_{2}$, and $^{1}/_{3}$ scale were experimented with. Resolved features on the 4 x 5 inch negatives and $^{2}/_{3}$ and $^{1}/_{2}$ scale 35 mm negatives were found to be insufficiently dense for mask usage. The $^{1}/_{3}$ scale 35 mm negatives was sufficiently dense for photolithography. A gold thin film was patterned using the 35 mm film at the $^{1}/_{3}$ scale size. Results are shown in Figures A.1 to A.4. It should be noted that the apparent curvature of these lines is due to the optics of the microscope used to take this picture and not due to the photographic reduction.

Comparing Figures A.1 to A.4 to Figures 3.1 to 3.4, it is seen that the resulting features are of poor quality and possess rougher edges. These rough edges can result in localized filling in of the spacings between features. Photo-reduction seems unable to produce good quality lines narrower than 15 µm, making this technique no better than linotronic printing. A further problem with this technique is that the photo-reduction step is performed manually. This has the possibility of introducing errors in the dimensionality of the mask image, and brings into question the repeatability of this mask making process. As the micro-Peltier device requires six masking layers for its fabrication, the process repeatability is of concern. This concern and the minimal resolution increase of the photo-reduction step lead to the abandonment of this mask making technique.

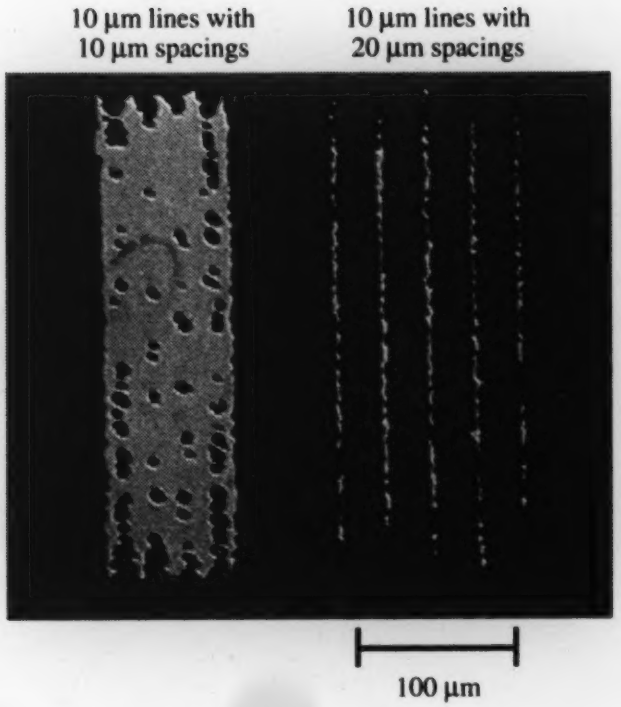

Figure A.1: Two sets of 10 µm lines patterned on thin film gold.

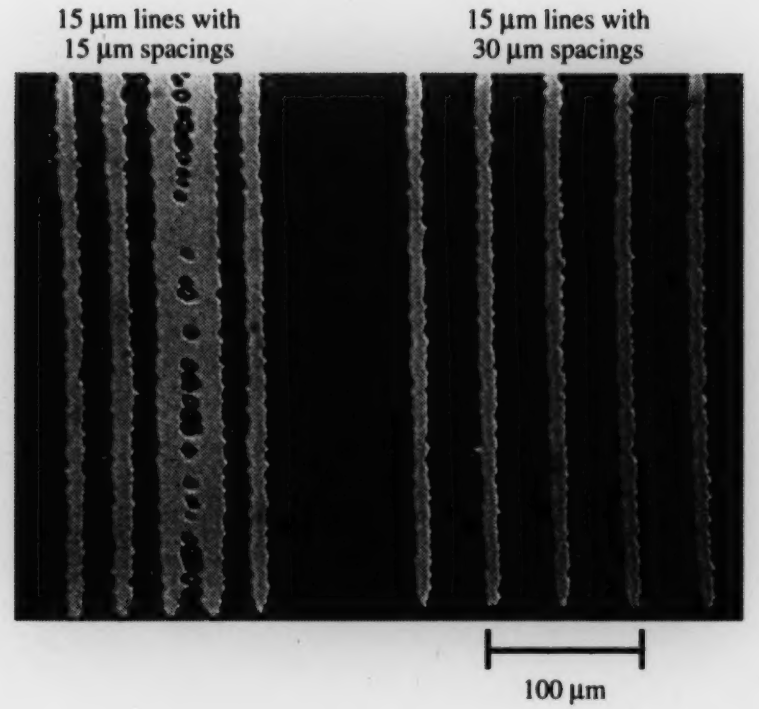

Figure A.2: Two sets of 15 µm lines patterned on thin film gold.

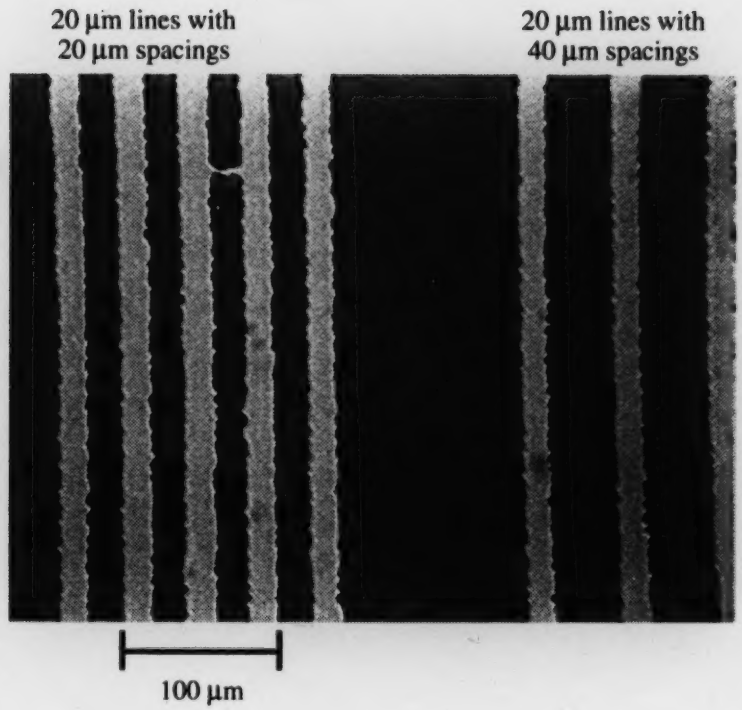

Figure A.3: Two sets of 20 µm lines patterned on thin film gold.

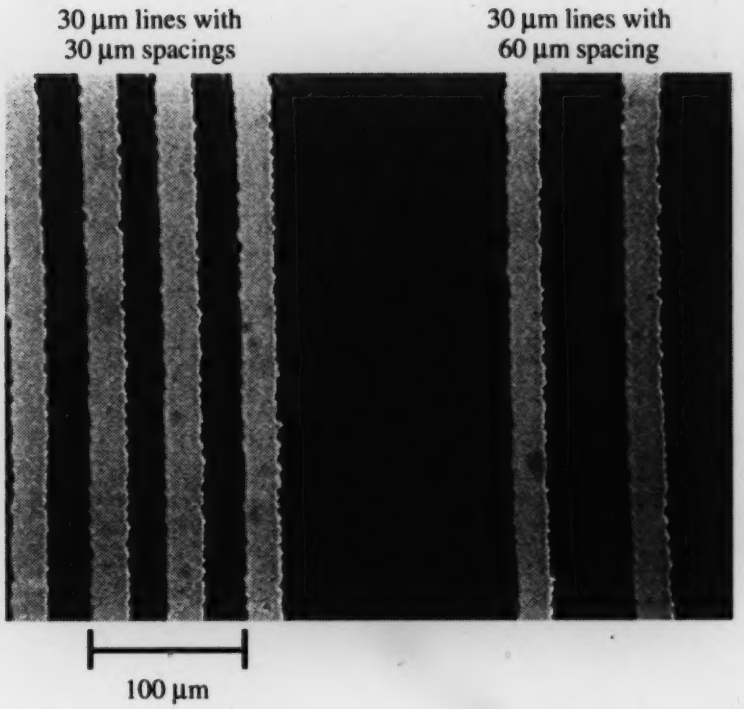

Figure A.4: Two sets of 30 µm lines patterned on thin film gold.

3.2.4 Photographic Slides As Masks

Direct printing of mask designs onto 35 mm slides was also investigated. This was done by University of Alberta Graphic Design Services. The process involved a 35 mm 4000 dpi (6.35 µm) CRT screen to expose the slide. The image was "printed" onto the CRT screen from within the software package used to make the image. Mask designs formatted for 8.5 x 11 inch paper were printed onto the 35 x 24 mm slides representing an image reduction of 8x. Unfortunately, while the imaging system was capable of 4000 dpi (6.35 µm) resolution, few films possess this resolution. Consequently, the image quality is highly film dependent.

Kodak ISO 100 Ektachrome color slide film was tested first, as this was the standard film used by Graphic Design Services. This film is only capable of 20 µm features according to Kodak technical support. Predictably, resulting images were of unacceptably poor resolution. Line images on the exposed slide could be resolved down to about 25 µm, but these lines were of poor quality. Smaller lines were of very poor quality. Furthermore, 10 - 15 µm inwards from the edge of each feature is an intermediate grayscale between black and white, making edge definition uncertain for photolithography.

Kodak TMAX-100 black and white film was also tested. As this is a negative film, the exposed image was color reversed. This film is capable of 5 µm features according to Kodak technical support. Results with this film were poor, with a final resolution not much better than the Ektachrome slide film. Furthermore, the TMAX negatives do not appear to be sufficiently opaque for use as photolithographic masks. Photolithography with these negatives was not attempted due to these characteristics.

The poor results with these films and the inability of this system to expose films slower than ISO 100 (films with lower ISO numbers possess higher resolution) resulted in this technique being abandoned.

Appendix B

ETCH-INDUCED STRESS FAILURE OF SiO_2 CANTILEVER BEAMS

B.1 Introduction

Stress in thin film microstructures was discussed in section 3.3.2. It was indicated that stress failures can occur when freeing a microstructure from the underlying silicon wafer. This type of failure is caused by the redistribution or concentration of stress during the etch of the underlying silicon when freeing micromechanical structures. During the release process, acute angles are often formed in the underlying silicon which can greatly concentrate stress in the above thin film microstructure. Such stress concentration may be sufficient to cause localized cracking of the microstructure (Figure B.1), even for relatively stress free dielectric thin films. Consequently, possible etch failure of a fabricated microstructure could very well be a function of its geometry (since its geometry controls the geometry of the silicon substrate etch), as opposed to the inherent stress in the thin film(s) making up the microstructure. Examples of etch induced stress failure during anisotropic silicon etching are shown in [B1-B2].

B.2 Cantilevers With Stress Failure

Micromachined 2.7 μm thick SiO_2 cantilevered beams were fabricated for this study. Low stress SiO_2 films were used in order to minimize the effect of non-etch induced stress on the failure of the cantilevered structures. PECVD SiO_2 films were deposited at 350°C on 3 inch <100> silicon wafers. The wafers were subsequently

annealed in a nitrogen ambient at 1100°C for 20 minutes in order to reduce stress in the SiO_2 film [26]. Stress levels before annealing were 2 x 10^9 dynes/cm^2 (200 MPa) compressive and 9.8 x 10^7 dynes/cm^2 (9.8 MPa) tensile after annealing, as measured by an Ionic Systems Stress Gauge (Model#30285). After annealing, the SiO_2 film was photolithographically patterned and etched in Buffered Oxide Etch (BOE) to form the cantilevers. The cantilevers were freed by anisotropic etch of the underlying silicon in a 33 % KOH solution at 80°C for 2 hours. A slow stir rate was achieved with a magnetic stir bar. After this etch, the wafers were gently rinsed in a low flow rate de-ionized water cascade (no-nitrogen bubble agitation) for 10 minutes to wash off the KOH etchant. The wafers were subsequently hung to air dry.

The length of KOH etch resulted in partial etching of the SiO_2 film. Exposed oxide etched at the rate of 37 Å /minute, removing 0.44 µm of SiO_2 over the 2 hours. It should also be noted that as the SiO_2 cantilever was freed, the exposed oxide was also attacked from the underside. Thus, the net oxide etch rate at the initial exposed edges of the cantilever was twice that at the base of the cantilever (which was not exposed to KOH attack from the underside until etch completion). A total of 0.88 µm of oxide was etched from the edges of the cantilever, giving the SiO_2 cantilevers a tapered thickness of 2.3 µm at their base and 1.8 µm at their edges.

Two cantilevers are shown in Figures B.2 and B.3. These cantilevers possess minimal curvature (indicating minimal inherent stress in the SiO_2 film), yet stress failures can be seen along the central axis of these cantilevers, originating at the triangular point formed by the exposed <211> crystal plane of the etched silicon. Due to the minimal inherent stress in the SiO_2 film, stress failures were not expected in these cantilevers. It was then suspected that the acute angle of the triangular point in the underlying etched silicon could be responsible for the observed failures.

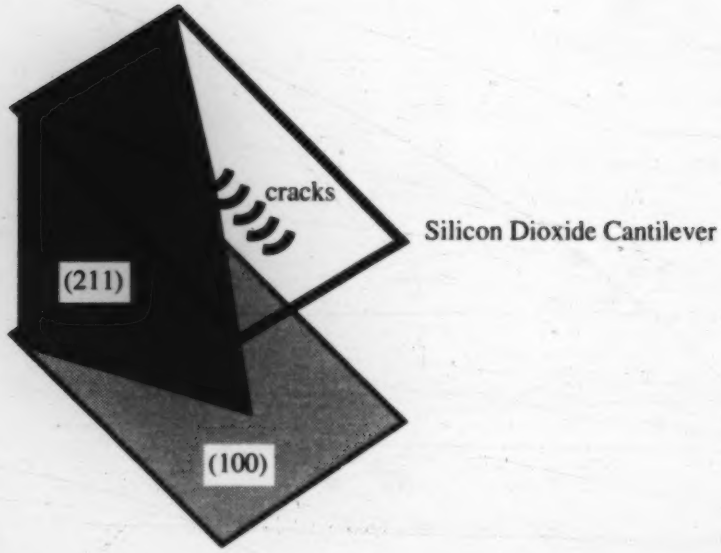

Figure B.1: Schematic of etch induced cracking of a SiO_2 cantilevered beam fabricated on a <100> silicon wafer. Cracks are centered with the triangular point formed by the <211> crystal plane.

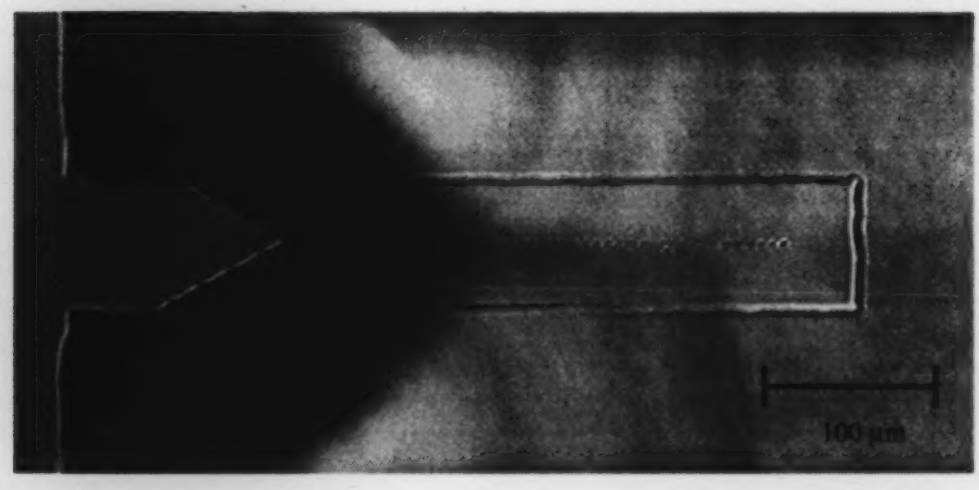

Figure B.2: Stress failures on a 460 x 80 µm SiO_2 cantilevered beam. A series of minor failures is seen to occur along the length of the beam.

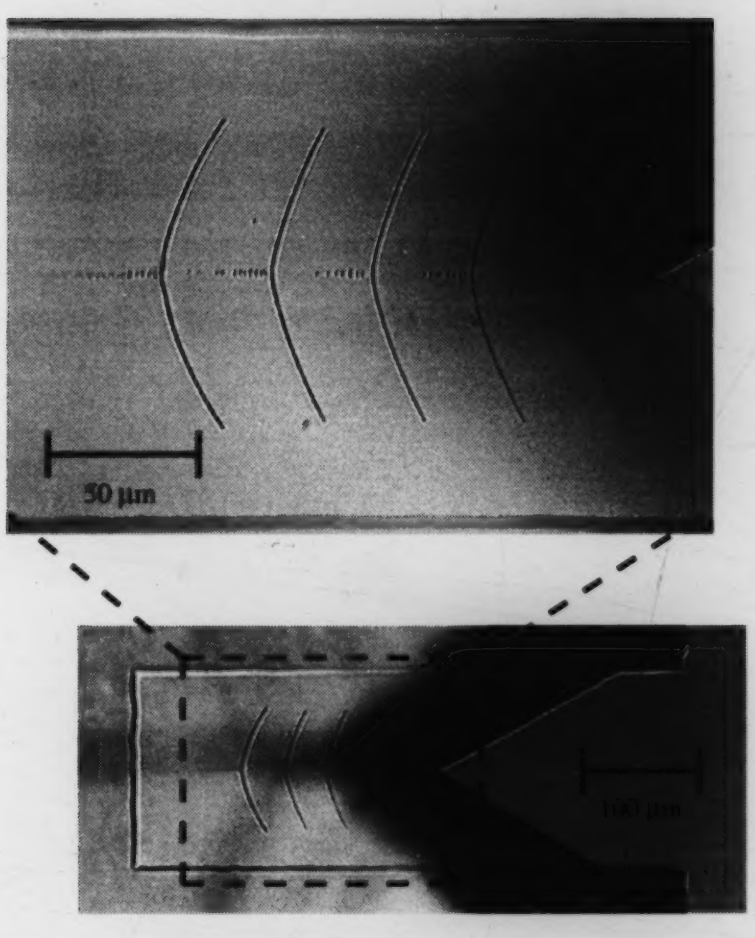

Figure B.3: Stress failures on a 460 x 180 µm SiO_2 cantilevered beam. Major crack failures are seen in this cantilever, along with a series of minor failures in advance of each of the major cracks.

Observation of the stress patterns of Figures B.2 and B.3 reveals the following. The 460 x 80 µm cantilever of Figure B.2 has a series of minor failures along its center axis. The wider cantilever of Figure B.3 (460 x 180 µm) possesses two types of failures. First, there are five major cracks which are equally spaced, similar in shape, and are

curved back toward the cantilever base. Second, there are a series of minor failures in advance of each of the major cracks.

The presence of major failures in the cantilever of Figure B.3 suggests that lower stress levels exist in the narrower cantilever of Figure B.2. It is also observed that failures are not seen close to the end of either cantilever, implying that the silicon substrate must be etched back some distance before the accumulated stress results in failure. These two observations suggest that the fabrication of shorter or narrower cantilevers are possible methods of preventing failure. In the cantilever of Figure B.3, no minor failures are seen to occur in close proximity to a major crack soon after the crack forms, indicating that the occurrence of a crack provides some degree of stress relief. The regular spacing of the cracks implies that the substrate must be etched back a given distance before the accumulated stress results in a major failure.

B.3 Stress Concentration During Etch

Stress in a thin film has two components [29]. The first is stress inherent in the thin film itself (intrinsic or in-plane stress). This component is strongly dependent on the deposition technique and conditions used in the deposition of the thin film. The second is differential stress characterized by the bending of the substrate-thin-film bi-layer due to differences in the thermal expansion coefficients of the substrate and thin film (thermal or bending stress).

The mechanism that gives rise to etch induced stress failures is related to mathematical stress singularities that can occur at re-entrant boundary corners, both for plane stress and plate bending problems [B3-B4]. In the case of the SiO_2 cantilevers of Figures B.2 and B.3, the boundary corner in question is where the cantilevers extend from the silicon wafer (line ABC in Figure B.4). Under mechanical loading of the cantilever, either in-plane or bending, a stress concentration would be expected at the re-entrant corner at point B. Although both in-plane and bending stresses exist in the cantilevers, the minimal curvature of the cantilevers themselves and nature of the major cracks of Figure B.3, suggest that it is the bending stress which dominates. This conclusion

agrees with the result for PECVD SiO_2 thin films found in [29].

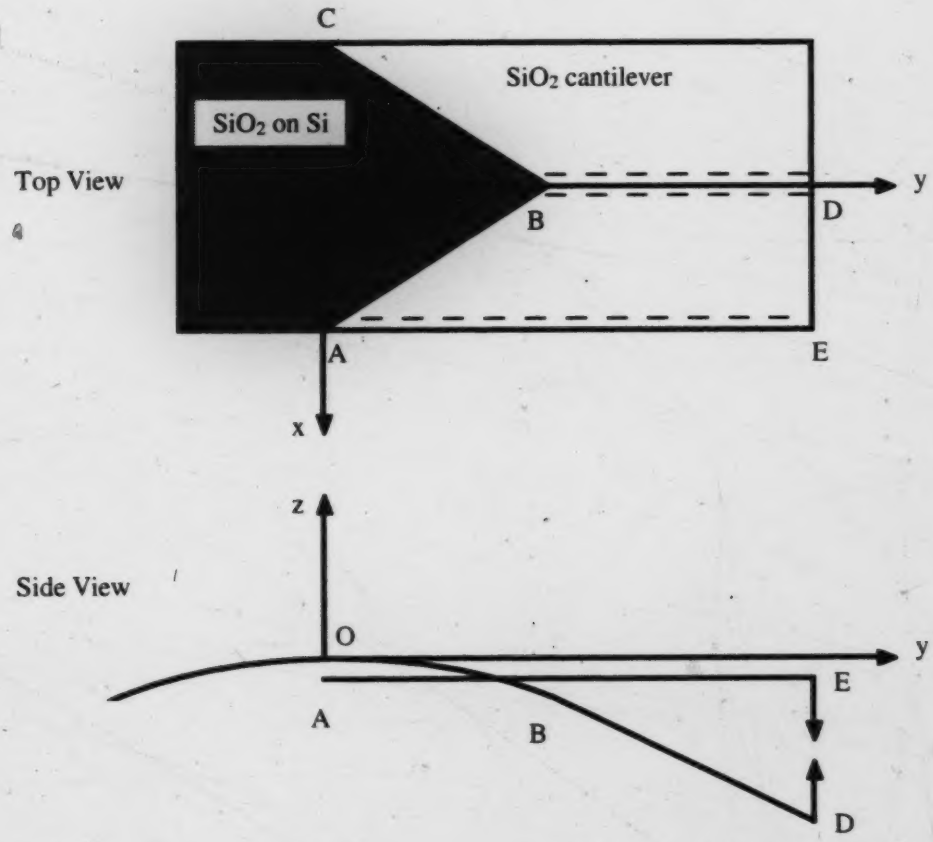

Figure B.4: Schematic of bending in the SiO_2 Cantilever.

To understand why the bending of the silicon-SiO_2 bi-layer concentrates stress in a cantilever during the etch of the underlying silicon, consider the longitudinal strips BD and AE shown in the partially freed cantilever of Figure B.4. Imagine the strips have been cut along the dashed lines, but remain attached at points A and B. Bending of the bi-layer causes the region to take on a spherical shape as indicated by the side view of line OB in Figure B.4. Taking point O as a reference point with zero displacement and rotation, point A moves down with no rotation in the yz plane. Point B moves a larger distance since it is further from O, and it undergoes a clockwise rotation about the x axis. The result is that if the strips were able to act independently (i.e. extend tangentially from points A and B), there would be considerable mismatch between the displacements at their free ends, points E and D.

In the case of the cantilever, the strips do not act independently. Thus, the tendency is for the outer strips to pull up on the inner strips and vise versa (as indicated by the arrows in Figure B.4). The result being that line DE takes on a curvature, which results in similar bending stress around point B to that caused by a load at D in the z direction. This "mechanical loading" of the cantilever during etch results in significant stress concentration at point B. This suggests that any potential failure of the cantilever during etch would occur at this location and is in agreement with the observed failures in Figures B.2 and B.3.

The curvature of line DE is demonstrated in Figures B.5 and B.6. Figure B.5 shows a silicon nitride (Si_3N_4) cantilever (250 μm long, 40 μm wide, 0.6 μm thick, deposited by PECVD at 350°C, etched in KOH for 3 hours to free it from the silicon substrate) extending from a silicon "peninsula" etched into the substrate. The cantilever itself shows little curvature, which is indicative of minimal inherent stress in the Si_3N_4 thin film. Figure B.6 shows a schematic of the top view of the structure. We can see that the front corners of the silicon peninsula were etched back during the KOH etch, freeing triangular Si_3N_4 overhangs. The leading edges of these overhangs correspond to the line segment DE of Figure B.4. It can be seen in Figure B.5 that these leading edges possess a bending curvature, validating the discussion of Figure B.4.

The above model suggests that the magnitude of the stress due to the loading of a cantilever during etch is greater for longer or wider cantilevers. This is due to a greater

bending displacement of the silicon-SiO_2 bi-layer with the increased distance. Accordingly, more significant etch induced stress failures would be expected in longer or wider cantilevers. This fact is shown experimentally in the narrow and wide cantilevers of Figures B.2 and B.3.

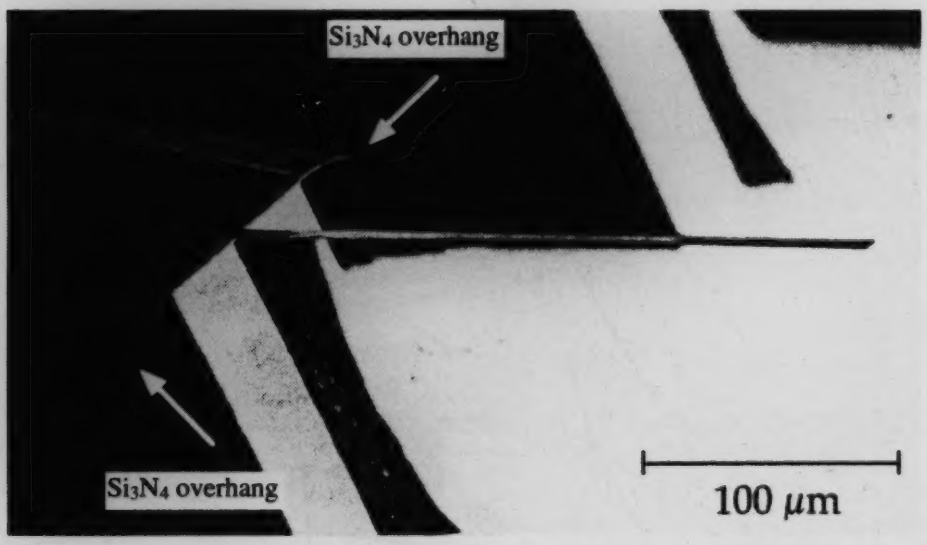

Figure B.5: A Si_3N_4 cantilever measuring 250 x 40 x 0.6 μm extending from a silicon peninsula etched into the substrate. The front corners of the silicon peninsula were etched back during the KOH etch, freeing triangular Si_3N_4 overhangs which are curved due to loading stress introduced by the substrate etch. The apparent narrowness of the cantilever results from the shallow viewing angle [B5].

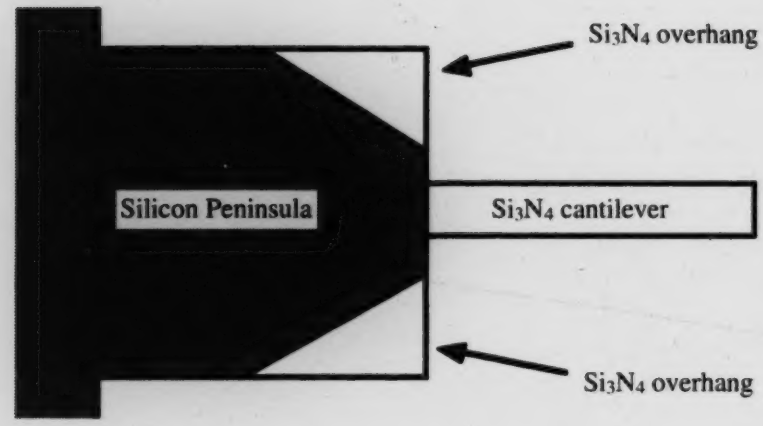

Figure B.6: A schematic of the top view of the structure of Figure B.5.

B.4 Analytical Stress Modelling

In order to substantiate the nature of the stress field predicted in the above paragraphs, an analytical model is used to demonstrate the nature of the stress field in a partially freed cantilever. A simple thermoelastic model is used, where a temperature change in a silicon-SiO_2 bi-layer is used to simulate bending stress in a cantilever. This model, shown in Figure B.7, consists of a SiO_2 cantilever plate extending tangentially from a Si-SiO_2 composite plate which is under curvature due to thermal expansion. Due to symmetry, an analysis can be performed on one half of the cantilever. The lateral dimensions in this model are representative of the cantilever of Figure B.3, as is the 2.5 μm thickness chosen for the SiO_2 layer. Details of this analysis are given in [B6] and will not be repeated here.

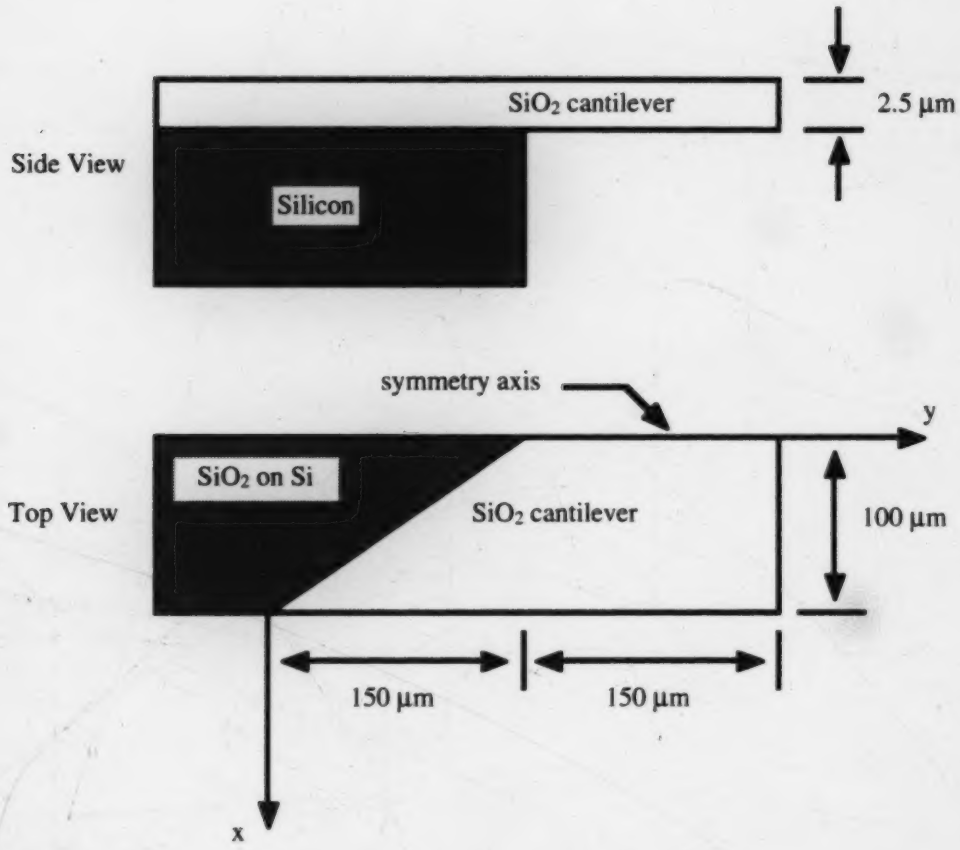

Figure B.7: Schematic of the geometry used for the finite element model.

Figure B.8 shows the probable vector direction failures would follow at each finite element node of the analytical model of [B6]. These vectors, which are normal to the direction of maximum principal stress, indicate that major crack failures would be expected to curve towards the cantilever base. This result qualitatively agrees with the direction of the observed major cracks in Figure B.3, suggesting that the described failure mechanism is consistent with the observed behavior.

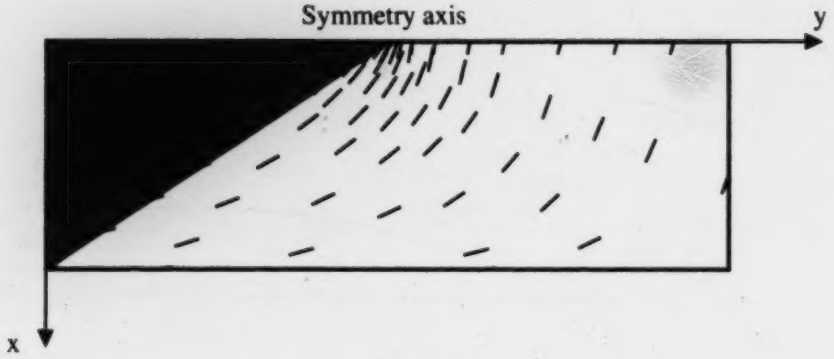

Figure B.8: Lines indicate the probable vector direction failures would follow at each finite element node of the analytical model.

The predictions of the analytical model suggest that the magnitude of the stresses in the cantilever in the vicinity of a sharp corner in the underlying silicon layer will increase as the length of the cantilever increases. Therefore, as the etching proceeds the stresses will build up until a major crack failure occurs. At that point the stresses drop suddenly, but will then start to increase again with further etching, eventually resulting in a subsequent crack failure. This is the origin of the regular spacing of the major crack failures seen in Figure B.3.

B.5 Avoiding Etch Induced Failures

The above discussion showed that cantilever failure is encouraged by stress concentration at acute angles formed in the underlying silicon substrate during etch. Therefore, it is reasonable to assume that cantilever failure could be avoided by etching the substrate in such a way as to preclude acute angle formation. This was found to be possible through the use of isotropic etching and by modification of the cantilever geometry.

B.5.1 Isotropic Etching

The use of an isotropic etchant in place of an anisotropic etchant for the silicon substrate etch is a possible method of avoiding failure. In an isotropic etch the underlying silicon is etched evenly from all sides (see Figure B.10). As the isotropic etch does not favor specific crystal planes in the silicon, the intersections of etch planes will not possess very sharp points. Accordingly, stress concentration at the intersection of etch planes is lessened.

SiO_2 cantilevers were fabricated using isotropic etching of the silicon substrate. A 1.7 μm SiO_2 thin film was deposited by PECVD at 350°C on a 3 inch <100> silicon wafer. After annealing in a nitrogen ambient at 1100°C for 20 minutes the stress level in the SiO_2 was measured to be 1.1 x 10^9 dynes/cm^2 (110 MPa) compressive. The SiO_2 film was photolithographically patterned and etched in BOE to form the cantilevers. The underlying silicon was etched by isotropic etch in a SF_6 plasma at 20 % flow, a pressure of 300 mTorr, and a power of 400 Watts. Plasma etching was chosen out of convenience. It is expected that isotropic wet etchants would show similar results. Resulting cantilevers are shown in Figures B.10 - B.12.

Isotropic etched cantilevers shown in Figures B.11 and B.12 possess no visible failure along their central axis, while cantilevers fabricated by anisotropic KOH etching from wafers of the same batch as Figures B.10 - B.12 showed similar failure to the cantilevers of Figures B.2 and B.3. The lack of visible failure in Figures B.11 and B.12 is notable as the stress level in the SiO_2 was 1.1 x 10^9 dynes/cm^2 (110 MPa) compressive, significantly higher than the 9.8 x 10^7 dynes/cm^2 (9.8 MPa) tensile stress level of the anisotropic etched cantilevers of Figures B.2 and B.3.

A potential problem with isotropic etching is undercutting of the silicon at the base of the cantilever. This undercut results in the etched silicon converging to a sharp point (see Figure B.12). Furthermore, undercut of the silicon to the sides of the cantilever base results in a "virtually wider" cantilever as seen by the sharp point at the cantilever base. These two factors result in significant stress concentration at the sharp undercut point. Consequently, failure may occur at this locality. Indeed, cracking is observed at this location in the cantilever of Figure B.12. This suggests caution when considering the

placement of devices or metallization in close proximity to this location.

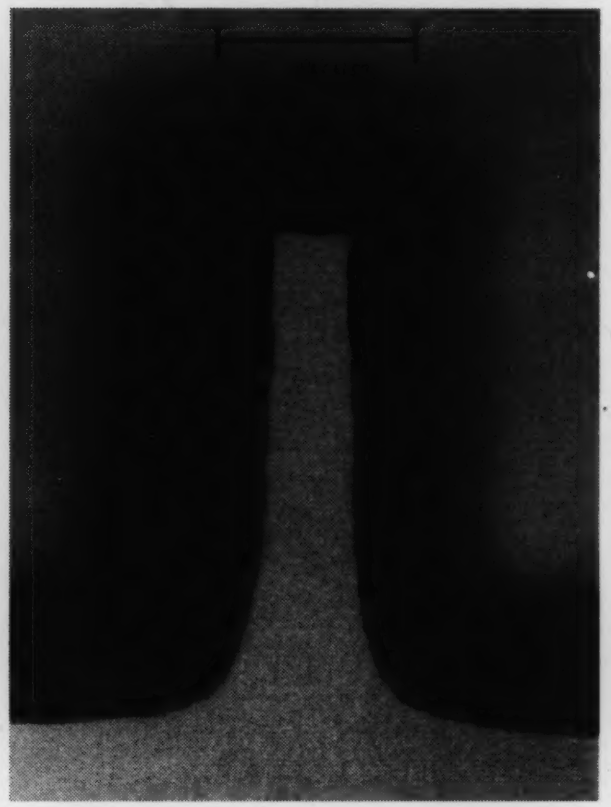

Figure B.10: A partially freed SiO_2 cantilever (255 x 180 μm) etched by isotropic plasma etching of the silicon substrate.

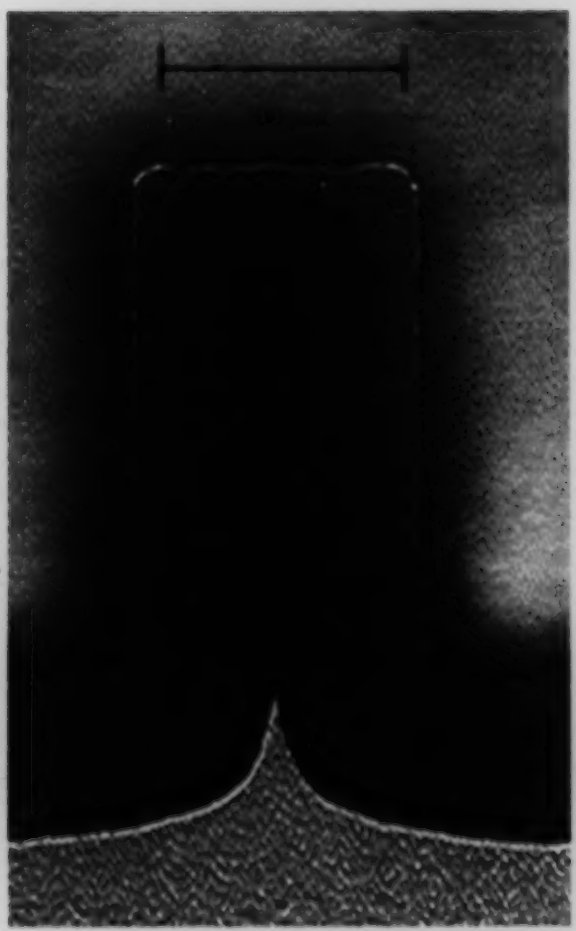

Figure B.11: A 210 x 120 µm SiO_2 cantilever formed by isotropic plasma etching of the underlying silicon.

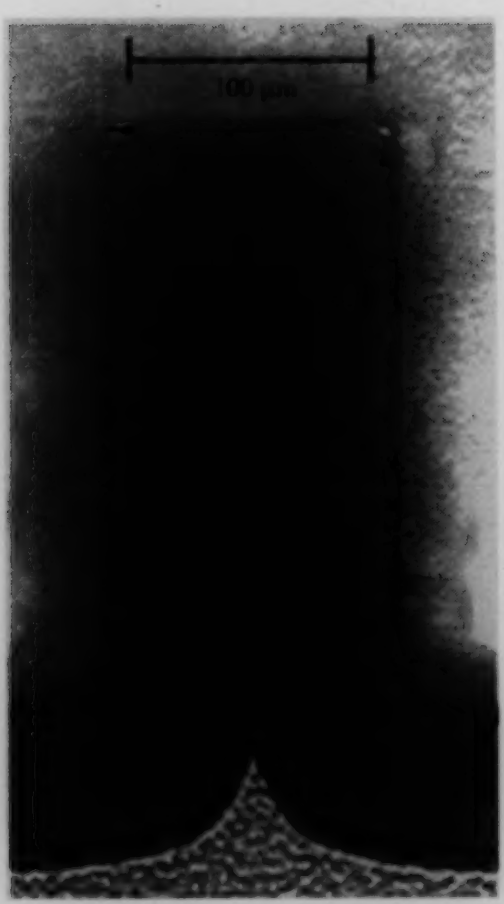

Figure B.12: A 240 x 120 µm SiO_2 cantilever etched by isotropic plasma etching of the silicon substrate. A crack failure can be seen at the apex of the sharp point at the base of the cantilever.

B.5.2 Modification OF Etch Geometry

In situations were anisotropic etchants are preferred, failures have been avoided by fabricating "antlers" at the end of cantilevers [B1]. During etch, the antlers hold the cantilever flat, preventing loading at the acute angle point formed in the etched silicon beneath the cantilever. This design requires careful dimensional design of the antlers, as they are required to etch free of the silicon substrate soon before the cantilever itself is etched free [B1].

An alternative design is to fabricate cantilevers with "ribs" along their sides. The presence of ribs modify the etch geometry of the silicon substrate in such a way as to prevent acute angle formation. Figure B.13 shows a 450 x 180 μm cantilever with ribs on its sides which successfully prevented stress related cracking. The SiO_2 thin film used for this cantilever was deposited using the same process used for the SiO_2 of Figures B.10 - B.12. Anisotropic etching was performed in a 33 % KOH solution at 80°C for 2 hours.

Cantilevers possessing similar dimensions to that of Figure B.13 which lacked ribs, showed etch induced stress failure similar to the cantilever of Figure B.3. Figure B.14 shows a cantilever possessing ribs only near its end. Cracking can be seen near the cantilever base which is lacking ribs. Figure B.15 shows a cantilever with no ribs, and cracking can be seen in three locations on the cantilever. The crack at the end of cantilever is located at the point where the underlying silicon is first etched to a sharp point during its etch.

A third method of avoiding crack failures is to fabricate cantilevers without a middle, essentially fabricating two cantilevers side by side attached at their ends. Two examples of such "double cantilevers" are shown in Figures B.16. Figure B.17 shows crack failures at the end of a double cantilever possessing a joined end of sufficient length to result in crack failures. Figure B.18 shows an identical cantilever with ribs along the joined end preventing the failures found in Figure B.17.

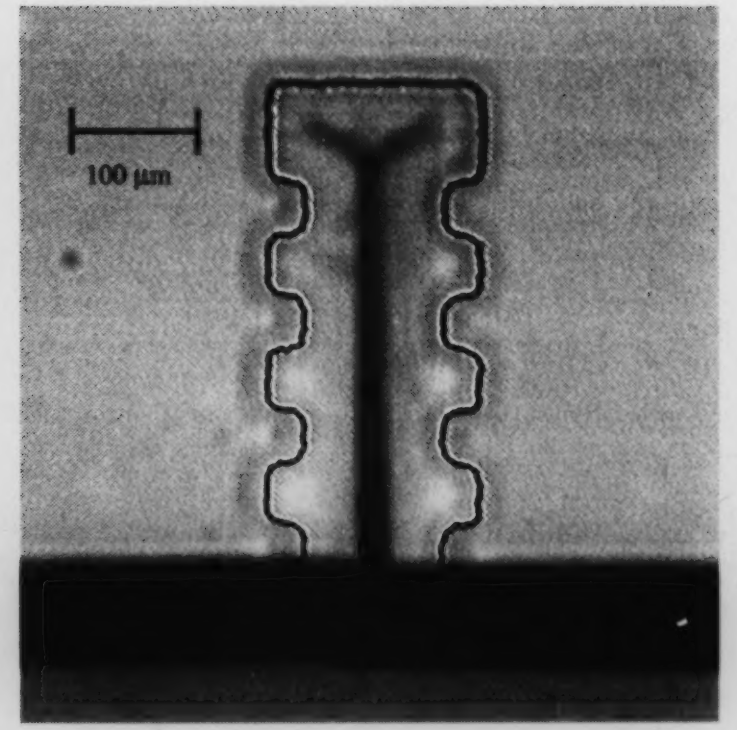

Figure B.13: A 450 x 180 µm cantilever with ribs on its sides. The ribs sufficiently prevented acute angle formation during etching, thus, avoiding stress related cracking.

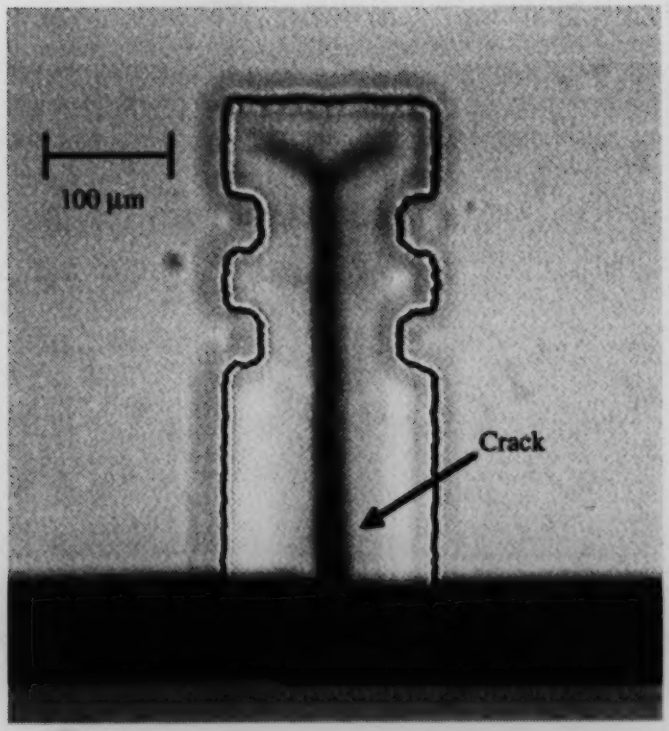

Figure B.14: A 450 x 180 µm cantilever with ribs only near its end. Cracking can be seen near the base of the cantilever which is lacking ribs.

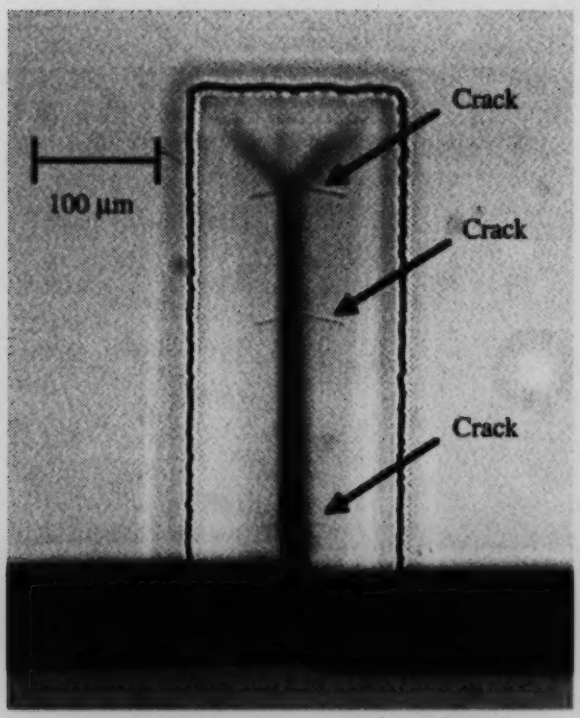

Figure B.15: A 450 x 180 µm cantilever with no ribs. Cracking is seen in three locations on the cantilever. The crack at the end of cantilever is located at the point where the underlying silicon is first etched to a sharp point during its etch.

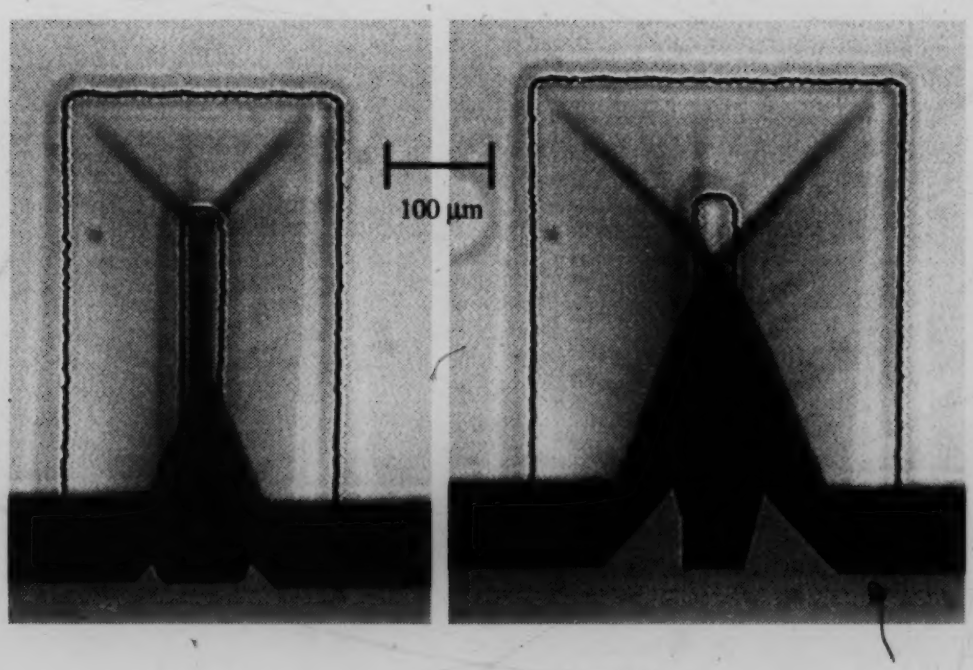

Figure B.16: Two 450 µm long double cantilevers.

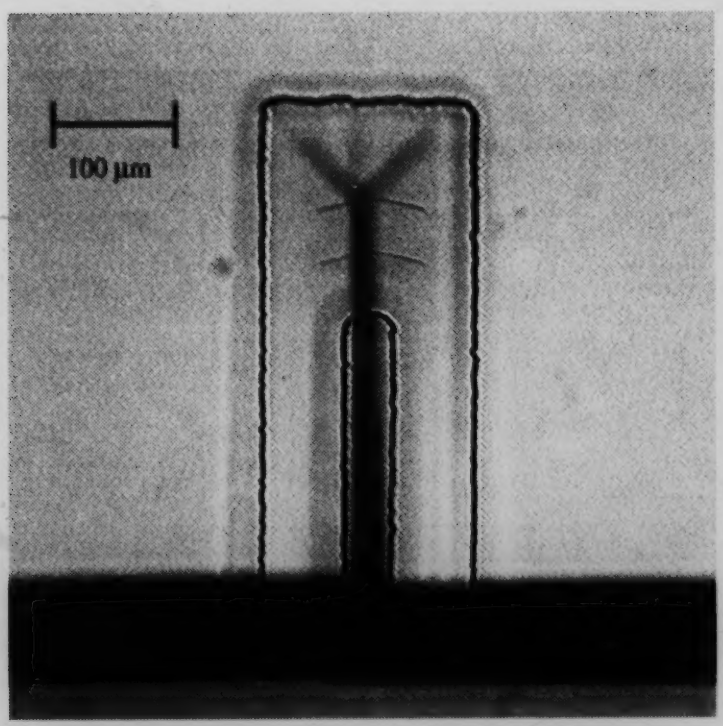

Figure B.17: A 450 µm long double cantilever. Cracking is seen within the elongated joined end of the cantilever.

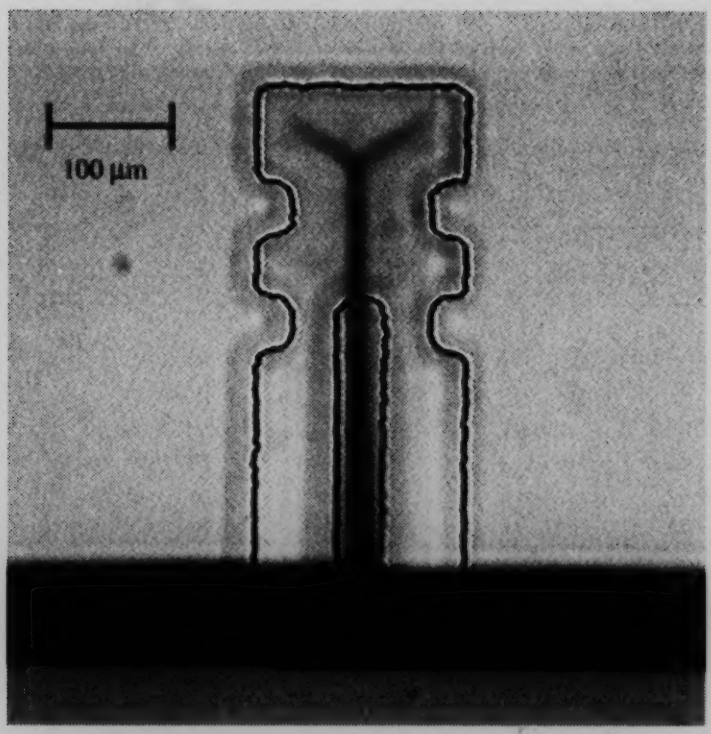

Figure B.18: A 450 µm long double cantilever. Ribs along the joined end prevented the failures found in Figure B.17.

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Appendix C

ASYMMETRIC BIPOLAR PULSED DC SPUTTERING OF SiO_2

C.1 Introduction

This section briefly discusses reactive asymmetric bipolar pulsed DC sputtering and experiments carried out on deposited SiO_2 thin films. Those unfamiliar with the sputtering process are referred to [C1].

C.2 Reactive Asymmetric Bipolar Pulsed DC Sputtering

Reactive asymmetric bipolar pulsed DC sputtering (I will call this RAPS for short.) was selected for the deposition of the SiO_2 passivation for the micro-Peltier device. This process was selected due to its faster rate of SiO_2 deposition in comparison to standard RF sputter deposition. In practice, the deposition rate for RAPS is between 60 - 70 % that of DC sputtering for the same metallic substrate [C2].

In a reactive sputtering process, oxygen gas reacts with silicon forming SiO_2 films on the substrate and on the silicon target. The SiO_2 "poisoned" layer on the silicon target acts as a dielectric material between the conductive plasma and target material. This forms a capacitor. Once this "parasitic capacitor" charges up to the DC sputtering voltage, no current flows through the target and so the sputtering process stops (Current flow is ion current. Therefore, if no argon ions strike the poisoned area, no sputtering of the target material occurs.).

RAPS eliminates target poisoning through the preferential sputtering of the SiO_2 layer on the target. This is achieved by the addition of a reverse bias pulse (say 100 V) to the normal DC voltage (say -400 V). This causes the parasitic capacitor to be charged to the opposite polarity of the applied reverse bias voltage (-100 V). When the voltage is switched back to sputter mode, the effective voltage on the plasma side of the parasitic capacitor is the sum of these two voltages (-500 V). Thus, the insulating target areas are preferentially sputtered away. It should be noted that the effectiveness of RAPS is also dependent on pulse frequency. Typical process frequencies are 80 kHz to 150 kHz. More information can be found on the RAPS process in [C2-C4].

C.3 Deposition And Etching Of Sputtered SiO_2 Films

Several SiO_2 films were deposited onto 3 inch <100> silicon wafers by the RAPS technique. Two sets of runs were performed with 4 wafers in each run. This was done to eliminate the variability factor of the sputtering system within each set of runs. Both pressure and gas concentration were varied during the depositions. All these films were deposited by Jim Broughton of the Alberta Microelectronic Centre. Results are shown in Tables C.1 and C.2.

Refractive index and film thickness measurements were performed using a prism coupler (Metricon, Model# 2010). Within each set of runs, it was observed that the deposition rate is faster at higher deposition pressures, except for wafer 3 of Run# 1. In runs 1 and 2, the refractive index of the sputtered SiO_2 films increased from 1.46 to 1.48 as the deposition pressures were decreased (An index of 1.46 is a good quality SiO_2 film.). In Run# 2, it is also seen that the refractive indexes were higher when lower oxygen concentrations were used. It should be noted that higher levels of arcing[1] were seen with decreasing deposition pressure. The arc count was in the hundreds for the

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[1] Arcing occurs across the parasitic capacitor formed by the SiO_2 layer on the silicon target. It is caused by dielectric breakdown of the insulating SiO_2 film in regions where the film is not strong enough to withstand the sputtering voltage.

lowest pressures (2.3 Torr). It is suspected that at lower pressures there is insufficient sputter removal of the SiO_2 during the reverse bias voltage cycle.

Etch rate measurements were performed to test the durability of the SiO_2 films and their acceptability for device processing. These tests were performed by coating select regions of a SiO_2 film with photoresist and dipping the sample into a solution of 10 : 1 BOE. After etch, the photoresist was removed, and the etch depth was measured with a profilometer (Tencor, Model® 10-200). In both runs 1 and 2, the etch rate appears to be lower when lower deposition pressures are used. In some cases, at the higher deposition pressures, the film "failed" over the regions unprotected by photoresist. That is to say, it was fully removed from the silicon wafer.

Annealing of the wafers in Run® 2 was performed at 600 °C for 30 minutes. The annealed films had no measurable change in thickness or refractive index. The annealed wafers also possessed slower etch rates, indicating a strengthening of the SiO_2 film.

Stress measurements were not done on the deposited films because the stress gauge was no longer operational.

C.4 Which Film Was Selected?

Etch tests conducted on the unannealed SiO_2 film deposited on wafer 4 of Run® 2 showed this film to be robust. Therefore, this film was selected as the passivation film for the micro-Peltier device.

Table C.1: Test results for Run# 1.

Process Conditions	Wafer 1	Wafer 2	Wafer 3	Wafer 4
Argon (%)	20	30	20	20
Oxygen (%)	7	7	7	7
Pressure (Torr)	6.6	8.5	5.2	2.8
$I_{initial}$ / $I_{15\ min}$ (amps)	1.58 / 1.68	1.78 / 1.69	1.71 / - -	1.56 / 1.51
Deposition Time	15 min	15 min	15 min	15 min
Film Thickness (μm)	1.44	1.70	1.45	1.19
Refractive Index	1.46	1.46	1.47	1.48
Etch Rate in 10 : 1 BOE (Å/min)				
- after a 1 minute etch	1110	failed	713	755
- after a 4 minute etch	failed	- -	survived	survived

Table C.2: Test results for Run# 2.

Process Conditions	Wafer 1	Wafer 2	Wafer 3	Wafer 4
Argon (%)	20	20	20	20
Oxygen (%)	7	7	5	5
Pressure (Torr)	5.2	2.3	5.2	2.3
$I_{initial}$ / $I_{15\ min}$ (amps)	1.49 / 1.55	1.29 / 1.24	1.10 / 1.13	0.89 / 0.89
Deposition Time	15 min	15 min	15 min	15 min
Film Thickness (μm)	1.34	1.07	1.23	0.876
Refractive Index	1.46	1.47	1.47	1.48
Etch Rate in 10 : 1 BOE (Å/min)				
- after a 1 minute etch	1357	950	failed	788
- after a 5 minute etch	failed	765	--	642
Etch Rate in 10:1 BOE (Å/min) after annealing for 30 minutes at 600 °C				
- after a 1 minute etch	880	733	1840	725
- after a 5 minute etch	failed	653	failed	636

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